

R7S72100 CPU (GENMAI) Optional Board

RTK7721000B00000BR

User's Manual

Renesas Microcomputer
RZ/A Series

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About This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the functions and operating specifications of this extension board. A basic knowledge of electrical circuits, logical circuits, and microcomputers (MCUs) is necessary in order to use this manual.

This manual is composed of an overview of the optional board; its functional and operational specifications.

Carefully read all notes described in the body of text in the manual.

The Revision History summarizes the modifications and additions to the previous versions. Refer to the text of the manual for details.

The following document applies to the R7S72100 CPU optional board RTK7721000B00000BR.

Document Type	Description	Document Title	Document No.
User's Manual	Describes functional specifications (devices, memory maps, electrical characteristics), and operational specifications (connectors, and switches)	R7S72100 CPU optional board RTK7721000B00000BR User's Manual	This publication

The following documents apply to the RZ/A1H group. Make sure to refer to the latest version of these documents which can be obtained from Renesas Electronics website.

Document Type	Description	Document Title	Document No.
Application note	Applications, sample programs, etc.	Available on Renesas Electronics website	
RENESAS TECHNICAL UPDATE	Information regarding product specifications, documents, etc.		

2. Frequently Used Abbreviations and Acronyms

ACIA	Asynchronous Communication Interface Adapter
bps	Bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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1. Overview

1.1 Overview

RTK7721000B00000BR is an optional board for the R7S72100 CPU board. The R7S72100 functions and its performance evaluation and the application software preceding development and evaluation can be executed by using the R7S72100 CPU board RTK7721000B00000BR. The features of the RTK7721000B00000BR are described below.

- Includes the following connectors to connect the TFT-LCD panel.
 - Alpha Project LCD-KIT-B01: 2
 - Renesas R0P7724LE0011RL: 1
 - General MIL connector: 40-pin×2
- Includes a video DAC and converts the TFT-LCD panel control signal to the analog RGB. The evaluation for the VDC5 display function can be executed by connecting to the monitor for PC.
- Includes general MIL connectors to evaluate the digital video signal input function (40-pin×1, 20-pin×1).
- Includes a 26-pin MIL connector to connect Aptina CMOS camera (MT9V024IA7XTCD ES)
- Includes audio DAC, CD deck interface, and key input switch which enable the preceding development for audio system.
- Includes UART connector, IrDA module, SIM card slot, LIN connector, and IEBus connector as the R7S72100 peripheral function interface.

1.2 System Configuration using RTK7721000B00000BR

Figure 1.2.1 shows the System Configuration using RTK7721000B00000BR.

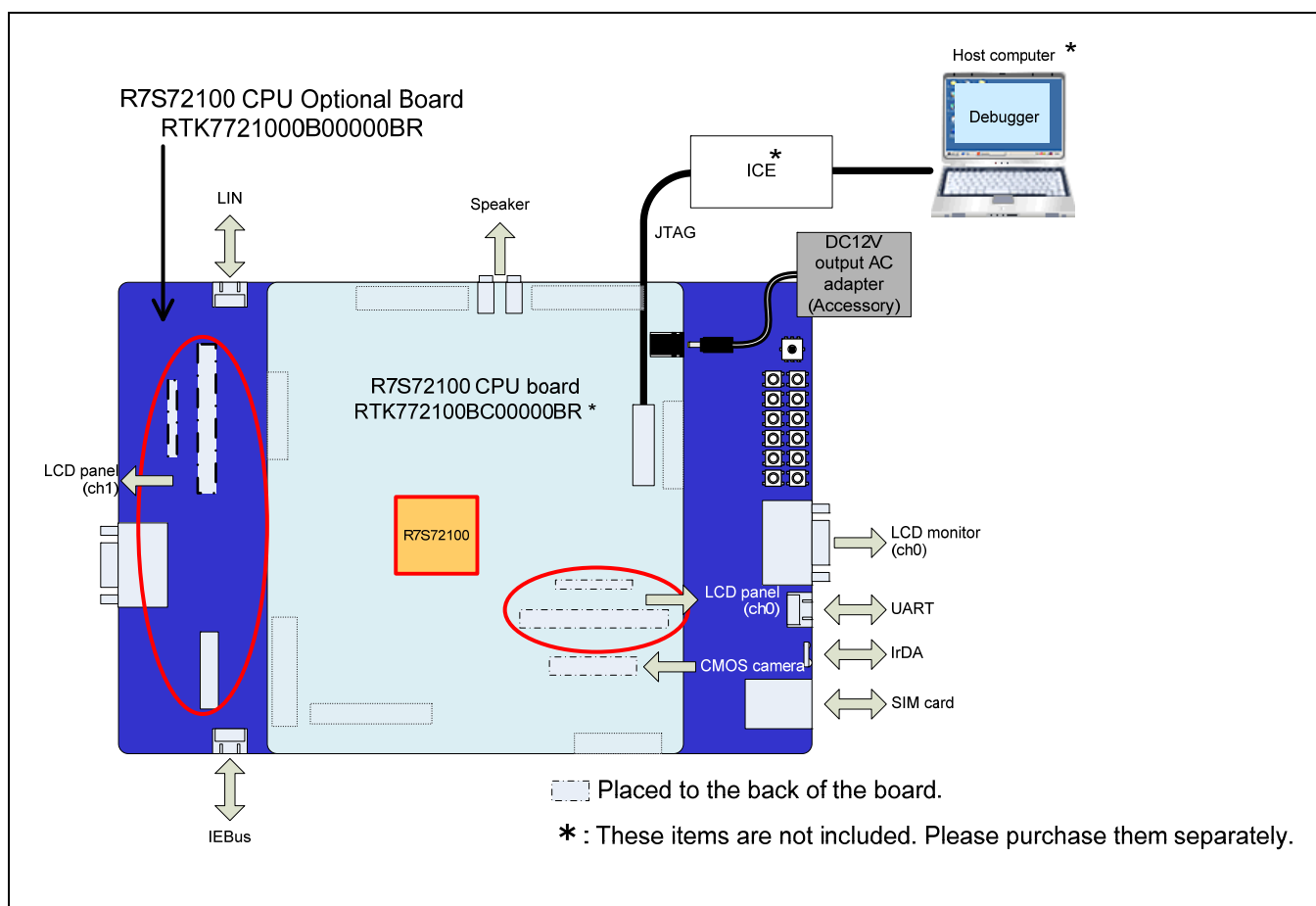


Figure 1.2.1 System Configuration using RTK7721000B00000BR

1.3 External Specifications

Table 1.3.1 lists the RTK7721000B00000BR External Specifications.

Table 1.3.1 RTK7721000B00000BR External Specifications

No.	Item	Description
1	TFT-LCD panel output	Includes three types of TFT-LCD panel connectors. • Alpha Project LCD-KIT-B01: 2 • Renesas R0P7724LE0011RL: 1 • General MIL standard connector: 40-pin×2
2	Analog RGB output	Converts digital RGB for TFT-LCD to analog RGB using Analog Devices video DAC (ADV7123). • Analog RGB connector: D-sub 15-pin connector×2
3	Digital video signal input	Includes digital video signal input connector for R7S72100 VDC5. • General MIL connector: 40-pin×1, 20-pin×1
4	connectors	• Lineout pin jacks (3.5 ϕ): 2 • SIM card slot • UART connector • LIN connector • IEBus connector • CD deck connector • HCI module connector • CMOS camera connector
5	Switches	• DIP switch for video DAC setting: 8/package×1 • DIP switch for key input: push switch×12, 4-directional switch with a center push type×1
6	Board specification	• Dimensions: 175×230mm • Mounting form: 6 layered, double-sided • Board thickness: 1.6mm • Number of board: 1

1.4 Exterior Appearance

Figure1.4.1 shows the RTK7721000B00000BR Exterior Appearance.

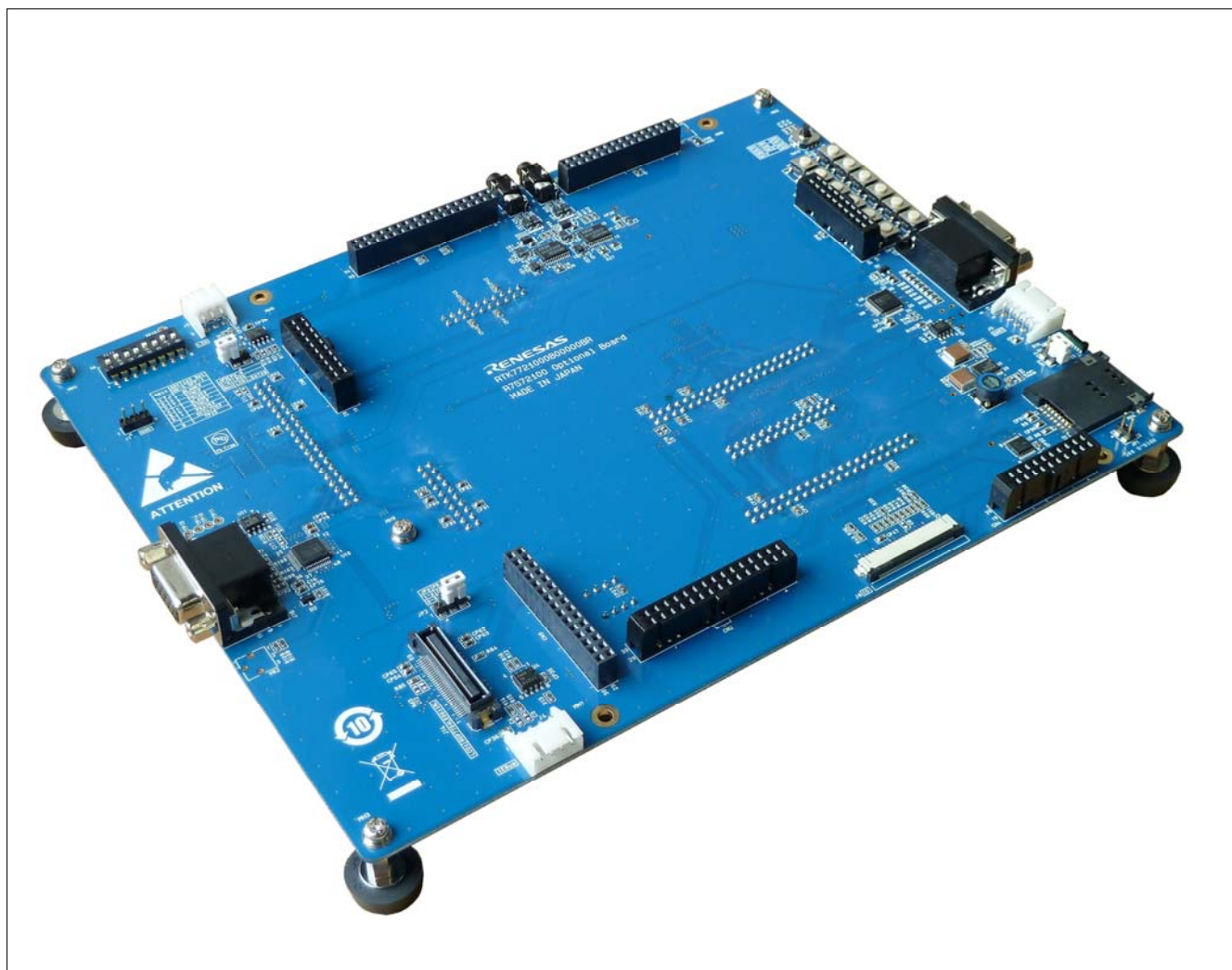


Figure1.4.1 RTK7721000B00000BR Exterior Appearance

1.5 Block Diagram

Figure1.5.1 shows the RTK7721000B00000BR Block Diagram.

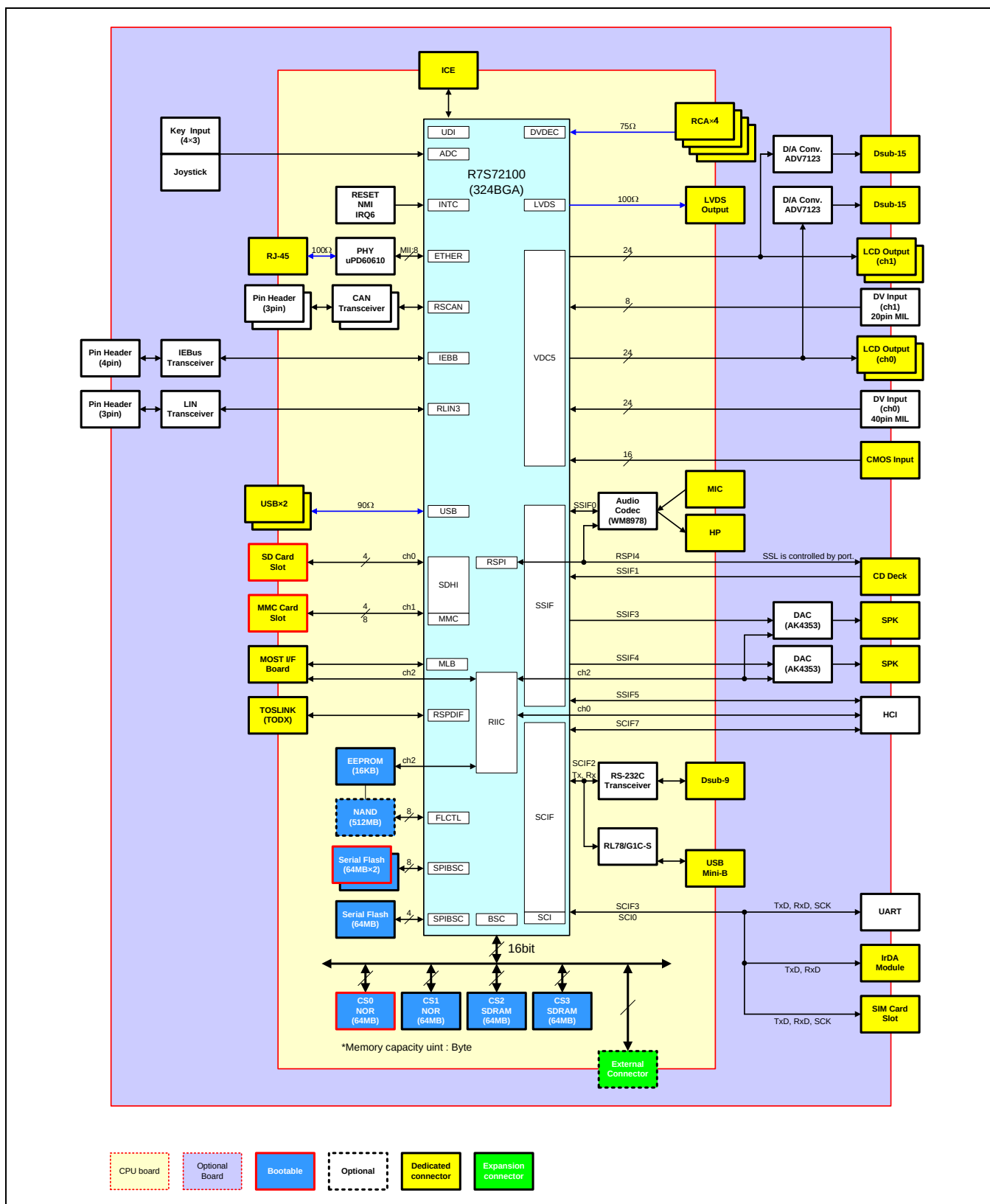


Figure1.5.1 RTK7721000B00000BR Block Diagram

1.6 Parts Layout

Figure1.6.1 and Figure1.6.2 show the Parts Layout of the RTK7721000B00000BR.

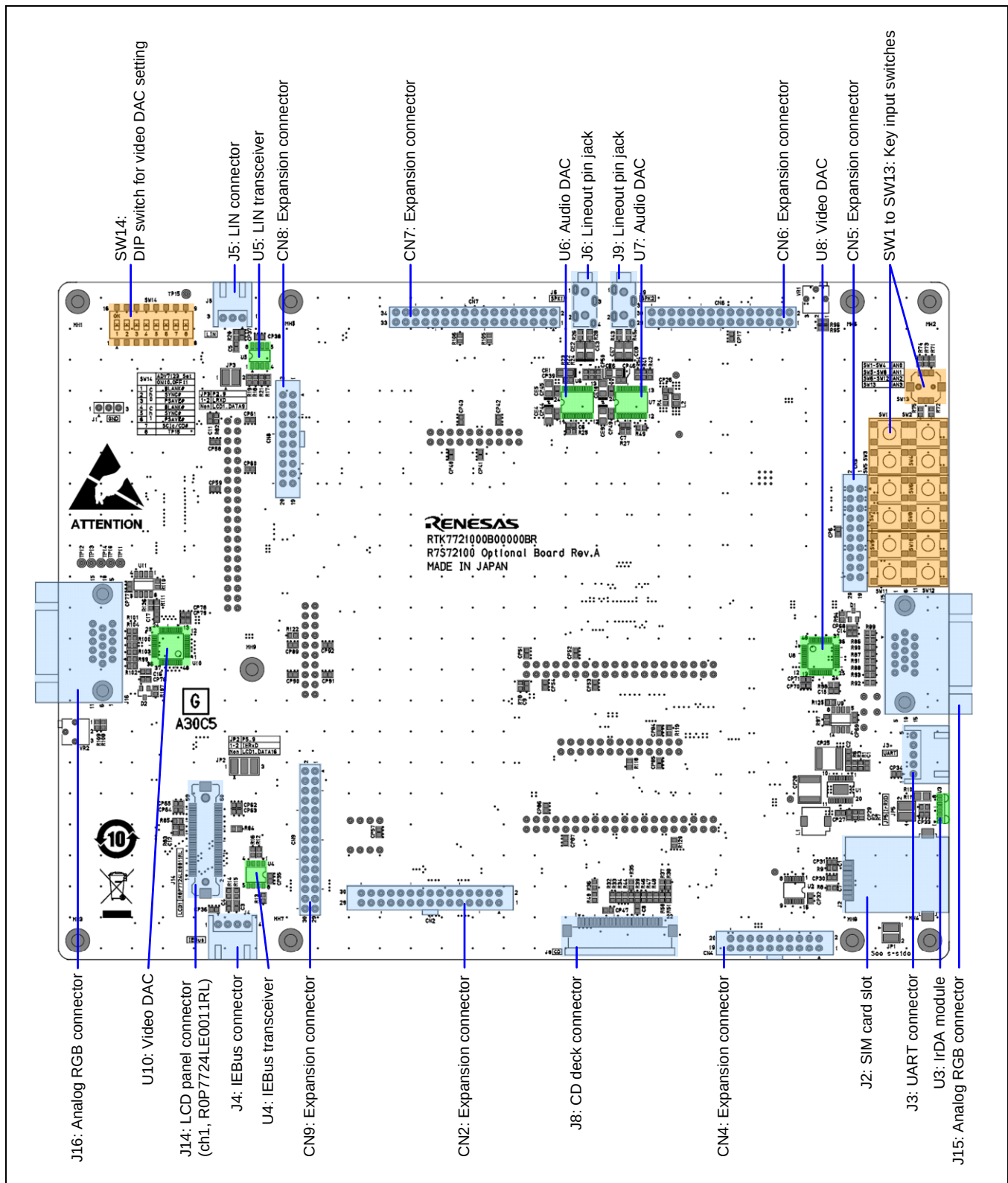


Figure1.6.1 RTK7721000B00000BR Parts Layout (Top View of Component Side)

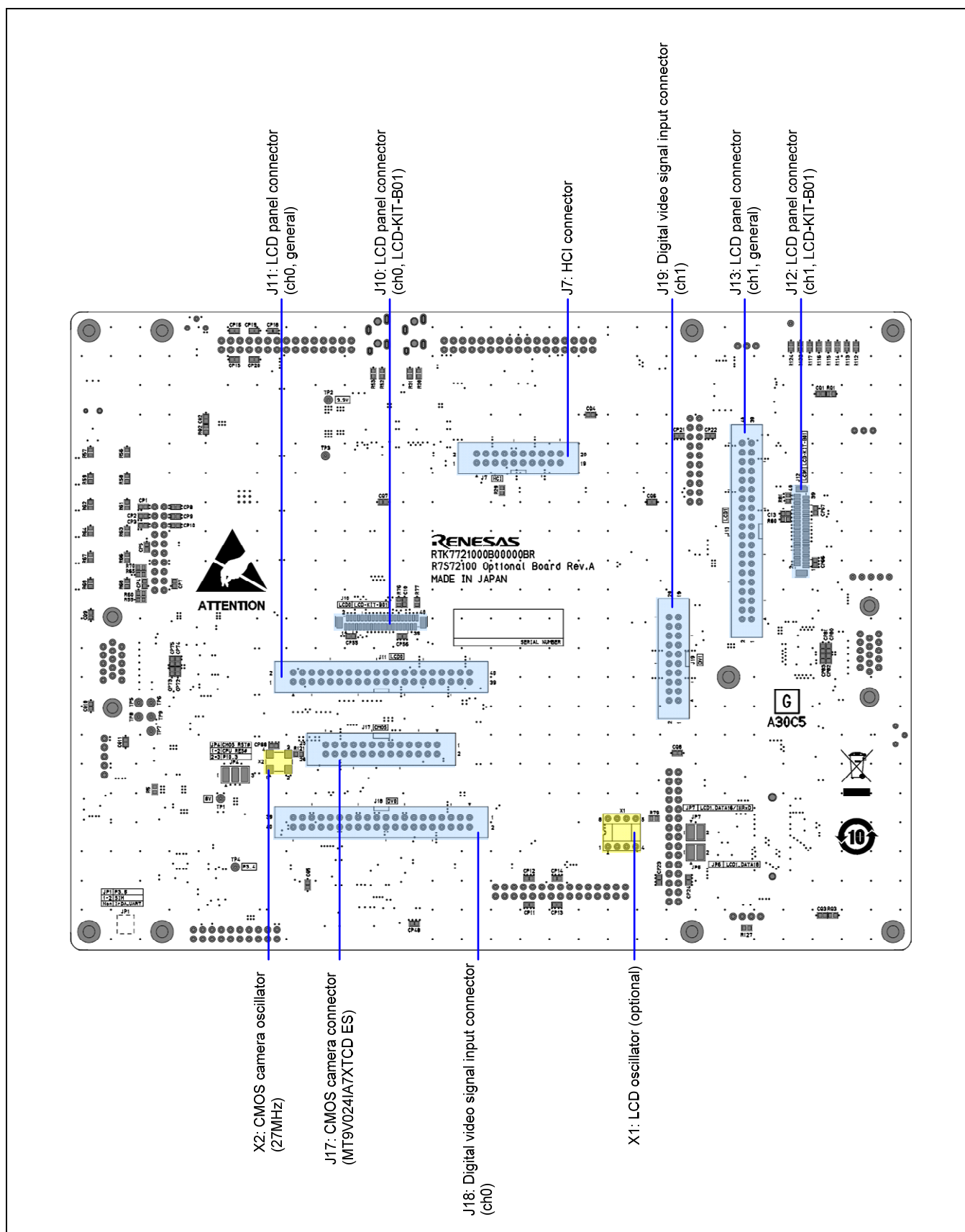


Figure1.6.2 RTK7721000B00000BR Parts Layout (Top View of Solder Side)

Table1.6.1 and Table1.6.2 list the main Parts of the RTK7721000B00000BR.

Table1.6.1 RTK7721000B00000BR Main Parts (1) IC

Part Number	Part Name	Type (Manufacturer)	Recommended Optional Parts
U1	8V regulator	LM20242 (TI)	12V → 8V
U3	IrDA module	RPM871 (ROHM)	
U4	IEBus transceiver	R2A11210SP (Renesas)	
U5	LIN transceiver	MAX13020 (Maxim)	
U6, U7	Audio DAC	AK4353VF (AKM)	
U8, U10	Video DAC	ADV7123 (Analog Devices)	
X2	CMOS camera oscillator	SG8002CA_27MHz (Epson)	

Table1.6.2 RTK7721000B00000BR Main Parts (2) Connectors

Part Number	Part Name	Type (Manufacturer)	Recommended Optional Parts
CN2	Expansion connector (30-pin)	HIF3FB-30DA-2.54DSA (HRS)	
CN4, CN5, CN8	Expansion connector (20-pin)	HIF3FB-20DA-2.54DSA (HRS)	
CN6, CN9	Expansion connector (30-pin)	SSW-115-01-L-D (Samtec)	
CN7	Expansion connector (34-pin)	SSW-117-01-L-D (Samtec)	
J2	SIM card slot	FMS006Z-2001-1 (Yamaichi)	
J3	UART connector	S5B-XH-A (JST)	
J4	IEBus connector	S4B-XH-A (JST)	
J5	LIN connector	S3B-XH-A (JST)	
J6, J9	Lineout pin jack	HSJ1456-010320 (Hoshiden)	
J7	HCI connector	HIF3FC-20PA-2.54DSA (HRS)	
J8	CD deck connector	IMSA-9617S-22Y922 (IRISO)	
J10, J12	LCD-KIT-B01 connector	XF2J-4024-12A (OMRON)	
J11, J13	General LCD connector	HIF3FC-40PA-2.54DSA (HRS)	
J14	R0P7724LE0011RL connector	8611-060S (KEL)	For ch1
J15, J16	Analog RGB output connector	XM4L-1542-132 (OMRON)	
J17	CMOS camera connector	N2526-6002RB (3M)	
J18	Digital video signal input connector (40-pin)	HIF3FC-40PA-2.54DSA (HRS)	For ch0
J19	Digital video signal input connector (20-pin)	HIF3FC-20PA-2.54DSA (HRS)	For ch1

1.7 Absolute Maximum Ratings

Table1.7.1 lists the RTK7721000B00000BR Absolute Maximum Ratings.

Table1.7.1 RTK7721000B00000BR Absolute Maximum Ratings

Symbol	Item	Value	Remarks
12Vcc ^{*1}	12V system power supply voltage	-0.3V to 15V	Vss reference
5Vcc ^{*1}	5V system power supply voltage	-0.3V to 6.25V	Vss reference
3Vcc ^{*1}	3.3V system power supply voltage	-0.3V to 4.6V	Vss reference
AVcc ^{*1}	Analog 3.3V system power supply voltage	-0.3V to 4.6V	AVss reference
T _{opr}	Operating ambient temperature ^{*2}	0°C to 50°C	Do not expose to condensation or corrosive gases.
T _{stg}	Storage ambient temperature ^{*2}	-10°C to 60°C	Do not expose to condensation or corrosive gases.

[Note] ^{*1} Supplied from R7S72100 CPU board.

^{*2} The ambient temperature is the air temperature immediate to the board.

1.8 Operating Conditions

Table1.8.1 lists the RTK7721000B00000BR Operating Conditions.

Table1.8.1 RTK7721000B00000BR Operating Conditions

Symbol	Item	Value	Remarks
12Vcc ^{*1}	12V system power supply voltage	10.8V to 13.2V	Vss reference
5Vcc ^{*1}	5V system power supply voltage	4.5V to 5.5V	Vss reference
3Vcc ^{*1}	3.3V system power supply voltage	3.0V to 3.6V	Vss reference
AVcc ^{*1}	Analog 3.3V system power supply voltage	3.0V to 3.6V	Vss reference
-	Maximum consumption voltage	Up to 3A	Includes R7S72100 CPU board consumption current
T _{opr}	Operating ambient temperature ^{*2}	0°C to 40°C	Do not expose to condensation or corrosive gases.

[Note] ^{*1} Supplied from R7S72100 CPU board.

^{*2} The ambient temperature is the air temperature immediate to the board.

2. Functional Specification

2.1 Functions Overview

Table2.1.1 lists the RTK7721000B00000BR Function Modules.

Table2.1.1 RTK7721000B00000BR Function Modules

Section	Function	Description
2.2	CPU	R7S72100 pin functions used on RTK7721000B00000BR
2.3	IEBus Interface	Connect the R7S72100 IEBus controller (IEBB) and the IEBus driver.
2.4	LIN Interface	Connect the R7S72100 LIN/UART interface (RLIN3) and the LIN driver.
2.5	SIM Card Interface	Connect the R7S72100 serial communication interface (SCI) and the SIM card slot.
2.6	IrDA Module	Connect the R7S72100 serial communication interface (SCI) and the IrDA module.
2.7	UART Interface	Connect the R7S72100 serial communication interface (SCI) pin to the UART connector.
2.8	Audio Interface	- Connect the R7S72100 and the D/A converter. - Two 96KHz, 24-bit D/A converters are included.
2.9	CD Deck Interface	Connect the R7S72100 Renesas serial peripheral interface (RSPI) and serial sound interface (SSIF) and the CD deck.
2.10	HCI Module Interface	Connect the pins for the R7S72100 HCI module to the MIL connector.
2.11	LCD Panel Output Interface	- Include 5 connectors with 3 types for LDC panel connectors. - Alpha Project LCD-KIT-B01 connector (ch0 and ch1) - Renesas R0P7724LE0011RL connector (ch1 only) - General MIL standard connector (ch0 and ch1)
2.12	Analog RGB Output Interface	- Convert the digital RGB for LCD to analog RGB using Analog Devices video DAC (ADV7123) - Analog RGB connectors: D-sub 15-pin connector×2
2.13	Digital Video Signal Input Interface	- Include the digital video signal input connector for the R7S72100 VDC5. - General digital video signal input connector: Digital video signal input connector: 20/40-pin MIL standard connector
2.14	CMOS Camera Input Interface	- Connect the R7S72100 capture engine unit (CEU) and the CMOS camera input connector. - Aptina CMOS camera (MT9V024IA7XTCD ES) connector×1
2.15	Key Input	Connect the R7S72100 A/D converter (ADC) and the switches.
2.16	Power Configuration	Power configuration of the RTK7721000B00000BR
-	Operation specifications	Connectors, switches (described in Chapter 3)

2.2 CPU

2.2.1 R7S72100 Overview

The RTK7721000B00000BR is used by connecting with the R7S72100 CPU board RTK772100BC00000BR which has the 32-bit RISK microcomputer with the maximum CPU clock frequency 400MHz.

2.2.2 RTK7721000B00000BR Pin Functions

Table 2.2.1 to Table 2.2.14 show the RTK7721000B00000BR Pin Functions.

Table 2.2.1 RTK7721000B00000BR Pin Functions (1)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
A1	Vss				
A2	P6_4 / D4 / LCD1_DATA12 / CRx2 / IRQ3 / RTS5 / RSPCK1 / DV0_DATA20	D4	Data bus	CN1-15	
A3	P0_3 / MD_CLKS	MD_CLKS	Connected to DIPSW as a clock selection input.	-	SW1-5
A4	P11_0 / DV0_DATA12 / TIOC4A / SCK6 / LCD0_DATA7 / VIO_D12	DV0_DATA12	Connected to DV0 input connector	CN9-28	
		LCD0_DATA7	Connected to LCD0 output connector		
		VIO_D12	Connected to CMOS camera input connector		
A5	P9_6 / LCD1_DATA22 / SPBIO20_0 / SSIWS2 / RTS1 / CS5	SPBIO20_0	Connected to serial flash memory 1	CN9-24	
		LCD1_DATA22	Connected to LCD1 output connector		
A6	P9_3 / LCD1_DATA19 / SPBSSL_0 / TxD1	SPBSSL_0	Connected to serial flash memory 1 and 2	CN9-19	JP7:Short
		LCD1_DATA19	Connected to LCD1 output connector		JP7:Open
A7	P5_9 / WE2/DQMUL / ET_MDC / DV0_VSYNC / IRQ2 / CRx1 / IERxD / LCD1_DATA16	ET_MDC	Connected to Ethernet PHY	CN9-16	JP4:2-3
		CRx1	Connected to CAN transceiver		JP7:Open
		IERxD	Connected to IEBus transceiver		JP4:1-2
		LCD1_DATA16	Connected to LCD1 output connector		JP4:Open
A8	Vss				JP2:1-2
A9	P5_6 / TXOUT0P / LCD1_DATA6 / LCD0_DATA22 / DV1_DATA6 / TxD6 / IRQ6 / SPDIF_IN / DV0_DATA14	TXOUT0P	Connected to LCD panel for LVDS	-	JP7:Short
		LCD1_DATA6	Connected to LCD1 output connector	CN9-8	
		DV1_DATA6	Connected to DV1 input connector		
A10	P5_2 / TXOUT2P / LCD1_DATA2 / LCD0_DATA18 / DV1_DATA2 / SCK3 / TIOC1B / MOSI3	TXOUT2P	Connected to LCD panel for LVDS	-	
		LCD1_DATA2	Connected to LCD1 output connector	CN9-4	
		DV1_DATA2	Connected to DV1 input connector		
A11	P5_0 / TXCLKOUTP / LCD1_DATA0 / LCD0_DATA16 / DV1_DATA0 / TxD4 / TIOC0A / RSPCK3	TXCLKOUTP	Connected to LCD panel for LVDS	-	
		LCD1_DATA0	Connected to LCD1 output connector	CN9-2	
		DV1_DATA0	Connected to DV1 input connector		
A12	Vss				
A13	VIN2B		Composite video, blanking, and sync (CVBS) channel 1 input pin2	-	
A14	VDAVss				

■: 3.3V system power supply, ■: 1.18V system power supply, ■: GND, Letters in Red indicate CPU board setting.

Table 2.2.2 RTK7721000B00000BR Pin Functions (2)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
A15	VIN2A		Composite video, blanking, and sync (CVBS) channel 0 input pin2	-	
A16	P0_2 / MD_CLK	MD_CLK	Connected to DIPSW as a clock mode input	-	SW1-4
A17	P1_6 / SCL3 / DV1_VSYNC / IERxD / IRQ6 / VIO_D12 / DV0_DATA12	SCL3	Connected to LCD1 output connector	CN8-20	
		DV1_VSYNC	Connected to DV1 input connector		
A18	P1_3 / SDA1 / DV0_DATA19 / ET_COL / IRQ3 / ADTRG	SDA1	Connected to TH7 of CPU board	CN8-15	
A19	P1_0 / SCL0 / DV0_DATA16 / TCLKA / IRQ0 / VIO_VD / DV0_VSYNC	SCL0	Connected to HCI connector Connected to LCD0 output connector Connected to CMOS camera input connector	CN8-14	
A20	P2_13 / D29 / SSL00 / DV0_DATA13 / SPBIO11_0 / CTx3 / SCK0 / LCD1_DATA13 / IRQ7	SPBIO11_0	Connected to serial flash memory 2	CN8-7	
		LCD1_DATA13	Connected to LCD1 output connector		
A21	P2_12 / D28 / RSPCK0 / DV0_DATA12 / SPBIO01_0 / CRx3 / IRQ6 / LCD1_DATA12 / TI0C1B	SPBIO01_0	Connected to serial flash memory 2	CN8-8	
		LCD1_DATA12	Connected to LCD1 output connector		
A22	Vss				
B1	Vcc				
B2	Vss				
B3	P6_0 / D0 / LCD1_DATA8 / LRXD0 / DV0_CLK / TI0C1A / IRQ5 / RxD3 / DV0_DATA16	D0	Data bus	CN1-20	
B4	P11_2 / DV0_DATA14 / TI0C4C / RxD6 / LCD0_DATA5 / VIO_D14	DV0_DATA14	Connected to DV0 input connector	CN9-30	
		LCD0_DATA5	Connected to LCD0 output connector		
		VIO_D14	Connected to CMOS camera input connector		
B5	P9_7 / LCD1_DATA23 / SPBIO30_0 / SSIDATA2 / TI0C1A	SPBIO30_0	Connected to serial flash memory 1	CN9-23	
		LCD1_DATA23	Connected to LCD1 output connector		
B6	P9_4 / LCD1_DATA20 / SPBIO00_0 / RxD1	SPBIO00_0	Connected to serial flash memory 1	CN9-22	
		LCD1_DATA20	Connected to LCD1 output connector		
B7	P5_10 / WE3/DQMUU/AH / DV0_HSYNC / CTx1 / IETxD / LCD1_DATA17	P5_10	Connected to TH3	CN9-15	
		CTx1	Connected to CAN transceiver		
		IETxD	Connected to IEBus transceiver		
		LCD1_DATA17	Connected to LCD1 output connector		
B8	P5_8 / LCD0_EXTCLK / IRQ0 / DV1_CLK / DV0_CLK / CS2	CS2	Connected to CS pin of SDRAM2	CN9-11	X1 (optional)
		LCD0_EXTCLK	Connects external clock for LCD panel		
B9	P5_7 / TXOUT0M / LCD1_DATA7 / LCD0_DATA23 / DV1_DATA7 / RxD6 / TI0C0D / SPDIF_OUT / DV0_DATA15	TXOUT0M	Connected to LCD panel for LVDS	-	
		LCD1_DATA7	Connected to LCD1 output connector	CN9-7	
		DV1_DATA7	Connected to DV1 input connector		
B10	P5_3 / TXOUT2M / LCD1_DATA3 / LCD0_DATA19 / DV1_DATA3 / TxD3 / TI0C3C / MISO3	TXOUT2M	Connected to LCD panel for LVDS	-	
		LCD1_DATA3	Connected to LCD1 output connector	CN9-3	
		DV1_DATA3	Connected to DV1 input connector		
B11	P5_1 / TXCLKOUTM / LCD1_DATA1 / LCD0_DATA17 / DV1_DATA1 / RxD4 / TI0C0B / SSL30	TXCLKOUTM	Connected to LCD panel for LVDS	-	
		LCD1_DATA1	Connected to LCD1 output connector	CN9-1	
		DV1_DATA1	Connected to DV1 input connector		
B12	Vss				

: 3.3V system power supply,
 : 1.18V system power supply,
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Table 2.2.3 RTK7721000B00000BR Pin Functions (3)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
B13	VIN1B		Composite video, blanking, and sync (CVBS) channel 1 input pin 1	-	
B14	VDAVcc				
B15	VIN1A		Composite video, blanking, and sync (CVBS) channel 0 input pin 1	-	
B16	P1_7 / SDA3 / DV1_HSYNC / LRXD0 / IRQ7 / VIO_D13 / DV0_DATA13	SDA3	Connected to LCD1 output connector	CN8-19	
		DV1_HSYNC	Connected to DV1 input connector		
B17	P1_4 / SCL2 / DV0_CLK / CRx1 / IRQ4 / CAN_CLK	SCL2	Connected to EEPROM	CN8-18	
			Connected to MOST I/F connector		
			Connected to DAC (AK4353) 1 and 2		
B18	P1_2 / SCL1 / DV0_DATA18 / FRB / IRQ2 / LCD1_EXTCLK	SCL1	Connected to TH6	CN8-16	
		FRB	Connected to NAND flash memory		
B19	P2_15 / D31 / MISO0 / DV0_DATA15 / SPBIO31_0 / CAN_CLK / RxD0 / LCD1_DATA15 / IRQ1	SPBIO31_0	Connected to serial flash memory 2	CN8-9	
		LCD1_DATA15	Connected to LCD1 output connector		
B20	PVcc				
B21	Vss				
B22	P2_10 / D26 / ET_RXD2 / DV0_DATA10 / SSIRxD0 / LTXD0 / LCD1_DATA10 / VIO_D10/MOSI4	ET_RXD2	Connected to Ethernet PHY	-	SW2-1:ON
		LTXD0	Connected to LIN connector	CN7-34	SW2-1:OFF
		LCD1_DATA10	Connected to LCD1 output connector		
C1	P6_5 / D5 / LCD1_DATA13 / CTx2 / SCK5 / SSL10 / DV0_DATA21	D5	Data bus	CN1-14	
C2	Vcc				
C3	Vss				
C4	P6_2 / D2 / LCD1_DATA10 / LRXD1 / IRQ7 / TCLKA / TIOC2A / RxD2 / DV0_DATA18	D2	Data bus	CN1-18	
C5	P11_3 / DV0_DATA15 / TIOC4D / LCD0_DATA4 / VIO_D15	DV0_DATA15	Connected to DV0 input connector	CN9-29	
		LCD0_DATA4	Connected to LCD0 output connector		
		VIO_D15	Connected to CMOS camera input connector		
C6	P11_1 / DV0_DATA13 / TIOC4B / TxD6 / LCD0_DATA6 / VIO_D13	DV0_DATA13	Connected to DV0 input connector	CN9-27	
		LCD0_DATA6	Connected to LCD0 output connector		
		VIO_D13	Connected to CMOS camera input connector		
C7	P9_5 / LCD1_DATA21 / SPBIO10_0 / SSISCK2 / CTS1 / CS4	SPBIO10_0	Connected to serial flash memory 1	CN9-21	
		LCD1_DATA21	Connected to LCD1 output connector		
C8	P9_2 / LCD1_DATA18 / SPBCLK_0 / LTXD0 / SCK1 / A0	SPBCLK_0	Connected to serial flash memory 1 and 2	CN9-20	JP6:Open
		LCD1_DATA18	Connected to LCD1 output connector		JP6:Short
C9	Vss				
C10	P5_5 / TXOUT1M / LCD1_DATA5 / LCD0_DATA21 / DV1_DATA5 / AUDIO_XOUT / TIOC0C / FCE / DV0_DATA13	TXOUT1M	Connected to LCD panel for LVDS	-	
		FCE	Connected to NAND flash memory	CN9-5	R110: mounted
		LCD1_DATA5	Connected to LCD1 output connector		
		DV1_DATA5	Connected to DV1 input connector		
C11	P5_4 / TXOUT1P / LCD1_DATA4 / LCD0_DATA20 / DV1_DATA4 / RxD3 / TIOC3D / DV0_DATA12	TXOUT1P	Connected to LCD panel for LVDS	-	
		LCD1_DATA4	Connected to LCD1 output connector	CN9-6	
		DV1_DATA4	Connected to DV1 input connector		
C12	LVDSAPVcc				

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Table 2.2.4 RTK7721000B00000BR Pin Functions (4)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
C13	VRM		A/D converter BOTTOM reference voltage pin for video signal input	-	
C14	REXT		A/D converter reference voltage pin for video signal input	-	22k $\Omega \pm 1\%$
C15	Vss				
C16	P1_5 / SDA2 / DV1_CLK / CRx4 / IRQ5 / VIO_CLK / LCD1_EXTCLK	SDA2	Connected to EEPROM	CN8-17	
			Connected to MOST I/F connector		
			Connected to DAC (AK4353) 1 and 2		
		DV1_CLK	Connected to DV1 input connector		
C17	P1_1 / SDA0 / DV0_DATA17 / TCLKC / IRQ1 / VIO_HD / DV0_HSYNC	SDA0	Connected to HCI connector Connected to LCD0 output connector Connected to CMOS camera input connector	CN8-13	
C18	P2_14 / D30 / MOSI0 / DV0_DATA14 / SPBIO21_0 / CRx4 / TxD0 / LCD1_DATA14 / IRQ0	SPBIO21_0	Connected to serial flash memory 2	CN8-10	
		LCD1_DATA14	Connected to LCD1 output connector		
C19	PVcc				
C20	Vss				
C21	P2_9 / D25 / ET_RXD1 / DV0_DATA9 / SSIWS0 / LRXD0 / LCD1_DATA9 / VIO_D9 / SSL40	ET_RXD1	Connected to Ethernet PHY	-	SW2-1:ON JP3:Open
		LRXD0	Connected to LIN connector	CN7-31	SW2-1:OFF JP3:Short
		LCD1_DATA9	Connected to LCD1 output connector		SW2-1:OFF JP3:Open
C22	P2_7 / D23 / ET_TXD3 / DV0_DATA7 / SSITxD5 / IETxD/RTS1 / VIO_D7 / LCD0_DATA23	ET_TXD3	Connected to Ethernet PHY	-	SW2-1:ON
		SSITxD5	Connected to HCI connector	CN7-29	SW2-1:OFF
D1	P6_7 / D7 / LCD1_DATA15 / LCD0_TCON6 / RxD5 / MISO1 / DV0_DATA23	D7	Data bus	CN1-12	
D2	P6_6 / D6 / LCD1_DATA14 / LCD0_TCON5 / TxD5 / MOSI1 / DV0_DATA22	D6	Data bus	CN1-13	
D3	Vcc				
D4	Vss				
D5	P6_3 / D3 / LCD1_DATA11 / LTXD1 / IRQ2 / CTS5 / TIOC2B / TxD2 / DV0_DATA19	D3	Data bus	CN1-17	
D6	P6_1 / D1 / LCD1_DATA9 / LTXD0 / IRQ4 / TIOC1B / SSIDATA4 / TxD3 / DV0_DATA17	D1	Data bus	CN1-19	
D7	PVcc				
D8	PVcc				
D9	LVDSPLLvcc				
D10	Vss				
D11	LVDSREFRIN			-	5.6k $\Omega \pm 1\%$
D12	LVDSAPVcc				
D13	Vcc				
D14	VRP		A/D converter TOP reference voltage pin for video signal input	-	
D15	Vss				
D16	PVcc				

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Table 2.2.5 RTK7721000B00000BR Pin Functions (5)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
D17	PVcc				
D18	PVcc				
D19	Vss				
D20	P2_8 / D24 / ET_RXD0 / DV0_DATA8 / SSISCK0 / LCD0_TCON6 / LCD1_DATA8 / VIO_D8 / RSPCK4	ET_RXD0	Connected to Ethernet PHY	-	SW2-1:ON
		LCD1_DATA8	Connected to LCD1 output connector	CN7-32	SW2-1:OFF
D21	P10_15 / DV0_DATA11 / SSITxD1 / MISO0 / LCD0_DATA8 / VIO_D11	DV0_DATA11	Connected to DV0 input connector	CN7-11	
		LCD0_DATA8	Connected to LCD0 output connector		
		VIO_D11	Connected to CMOS camera input connector		
D22	P10_14 / DV0_DATA10 / SSIRxD1 / MOSI0 / LCD0_DATA9 / VIO_D10	DV0_DATA10	Connected to DV0 input connector	CN7-12	
		LCD0_DATA9	Connected to LCD0 output connector		
		VIO_D10	Connected to CMOS camera input connector		
E1	P6_10 / D10 / DV0_DATA14 / LCD0_TCON5 / RxD0 / LCD0_DATA2 / IRQ2	D10	Data bus	CN1-8	
E2	P6_9 / D9 / DV0_DATA13 / TxD0 / LCD0_DATA1 / IRQ1	D9	Data bus	CN1-9	
E3	P6_8 / D8 / DV0_DATA12 / CAN_CLK / SCK0 / LCD0_DATA0 / IRQ0	D8	Data bus	CN1-10	
E4	Vcc				
E19	P2_11 / D27 / ET_RXD3 / DV0_DATA11 / SSITxD0 / TIOC1A / LCD1_DATA11 / VIO_D11 / MISO4	ET_RXD3	Connected to Ethernet PHY	-	SW2-1:ON
		P2_11	Connected to LIN connector (sleep control)	CN7-33	SW2-1:OFF
		LCD1_DATA11	Connected to LCD1 output connector		
E20	P2_6 / D22 / ET_TXD2 / DV0_DATA6 / SSIRxD5 / RxD1 / VIO_D6 / LCD0_DATA22	ET_TXD2	Connected to Ethernet PHY	-	SW2-1:ON
		SSIRxD5	Connected to HCI connector	CN7-30	SW2-1:OFF
E21	P10_12 / DV0_DATA8 / SSISCK1 / RSPCK0 / LCD0_DATA11 / VIO_D8	DV0_DATA8	Connected to DV0 input connector	CN7-10	
		LCD0_DATA11	Connected to LCD0 output connector		
		VIO_D8	Connected to CMOS camera input connector		
E22	P2_5 / D21 / ET_TXD1 / DV0_DATA5 / SSIWS5 / SPBSSL_1 / TxD1 / VIO_D5 / LCD0_DATA21	ET_TXD1	Connected to Ethernet PHY	-	SW2-1:ON
		SSIWS5	Connected to HCI connector	CN7-27	SW2-1:OFF
F1	P6_14 / D14 / DV0_DATA22 / TxD6 / LCD0_DATA6 / IRQ6	D14	Data bus	CN1-3	
F2	P6_13 / D13 / DV0_DATA21 / SCK6 / RXD1 / LCD0_DATA5 / IRQ5	D13	Data bus	CN1-4	
F3	P6_11 / D11 / DV0_DATA15 / LCD0_TCON6 / SCK1 / LCD0_DATA3 / IRQ3	D11	Data bus	CN1-7	
F4	Vcc				
F19	P2_4 / D20 / ET_TXD0 / DV0_DATA4 / SSISCK5 / SPBCLK_1 / SCK1 / VIO_D4 / LCD0_DATA20	ET_TXD0	Connected to Ethernet PHY	-	SW2-1:ON
		SSISCK5	Connected to HCI connector	CN7-28	SW2-1:OFF
F20	P10_13 / DV0_DATA9 / SSIWS1 / SSL00 / LCD0_DATA10 / VIO_D9	DV0_DATA9	Connected to DV0 input connector	CN7-9	
		LCD0_DATA10	Connected to LCD0 output connector		
		VIO_D9	Connected to CMOS camera input connector		

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Table 2.2.6 RTK7721000B00000BR Pin Functions (6)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
F21	P2_2 / D18 / ET_TXEN / DV0_DATA2 / SPBIO20_1 / MLB_SIG / TIOC2B / VIO_D2 / LCD0_DATA18	ET_TXEN	Connected to Ethernet PHY	-	SW2-1:ON
		MLB_SIG	Connected to MOST I/F connector	CN7-26	SW2-1:OFF
F22	P4_15 / LCD0_DATA23 / LCD1_TCON2 / SD_D2_0 / MMC_D2 / SPBIO31_1 / SSITxD3 / RxD2 / IRQ7	SD_D2_0	Connected to SD card slot	CN7-19	
		LCD1_TCON2	Connected to LCD1 output connector		
		SSITxD3	Connected to DAC (AK4353) 1		
G1	P11_13 / CTx1 / SSL10 / LCD0_TCON4 / MMC_D5 / LCD0_TCON1	LCD0_TCON1	Connected to LCD0 output connector	CN2-19	
G2	P11_12 / CRx1 / RSPCK1 / IRQ3 / MMC_D4 / LCD0_TCON2	LCD0_TCON2	Connected to LCD0 output connector	CN2-20	
G3	P6_15 / D15 / DV0_DATA23 / RxD6 / LCD0_DATA7 / IRQ7	D15	Data bus	CN1-2	
G4	P6_12 / D12 / DV0_DATA20 / TXD1 / LCD0_DATA4 / IRQ4	D12	Data bus	CN1-5	
G19	P4_14 / LCD0_DATA22 / LCD1_TCON1 / SD_D3_0 / MMC_D3 / SPBIO21_1 / SSIIRxD3 / TxD2 / IRQ6	SD_D3_0	Connected to SD card slot	CN7-20	
		LCD1_TCON1	Connected to LCD1 output connector		
		P4_14	Connected to DAC (AK4353) 1 and 2		
G20	P2_3 / D19 / ET_CRS / DV0_DATA3 / SPBIO30_1 / IERxD / CTS1 / VIO_D3 / LCD0_DATA19	ET_CRS	Connected to Ethernet PHY	-	SW2-1:ON
		P2_3	Connected to MOST I/F connector (reset control)	CN7-25	SW2-1:OFF
G21	P4_13 / LCD0_DATA21 / LCD1_TCON0 / SD_CMD_0 / MMC_CMD / SPBIO11_1 / SSIWS3 / RxD1 / IRQ5	SD_CMD_0	Connected to SD card slot	CN7-17	
		LCD1_TCON0	Connected to LCD1 output connector		
		SSIWS3	Connected to DAC (AK4353) 1		
G22	Vss				
H1	P7_2 / RAS / DV0_DATA18 / ET_TXER / RxD4 / CRx2 / SSIWS1 / TIOC0C	RAS	Connected to SDRAM 1 and 2	CN2-28	JP1:Open
		CRx2	Connected to CAN transceiver		JP1:Short
H2	P7_1 / CS3 / DV0_DATA17 / ET_TXCLK / TXD4 / DV0_CLK / SSISCK1 / TIOC0B	CS3	Connected to SDRAM 2	CN2-29	
H3	P11_14 / SPDIF_IN / MOSI1 / LCD0_TCON5 / MMC_D6 / LCD0_TCON0	LCD0_TCON0	Connected to LCD0 output connector	CN2-18	
H4	P7_0 / MD_BOOT2 / CS0 / DV0_DATA16 / ET_MDC / SCK4 / LTXD0 / TIOC0A	MD_BOOT2	Connected to DIPSW as a boot mode input	CN2-30	SW1-3
		CS0	Connected to NOR flash memory 1		JP5:1-2 JP5:2-3
H19	P4_11 / LCD0_DATA19 / LCD1_TCON6 / SD_D0_0 / MMC_D0 / SSITxD5 / CTx4 / SCK1 / IRQ3	SD_D0_0	Connected to SD card slot	CN7-15	
		LCD1_TCON6	Connected to LCD1 output connector		
H20	P10_11 / DV0_DATA7 / TIOC2B / ET_RXD3 / LCD0_DATA12 / VIO_D7	DV0_DATA7	Connected to DV0 input connector	CN7-7	
		LCD0_DATA12	Connected to LCD0 output connector		
		VIO_D7	Connected to CMOS camera input connector		
H21	P10_10 / DV0_DATA6 / TIOC2A / ET_RXD2 / LCD0_DATA13 / VIO_D6	DV0_DATA6	Connected to DV0 input connector	CN7-8	
		LCD0_DATA13	Connected to LCD0 output connector		
		VIO_D6	Connected to CMOS camera input connector		

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Table 2.2.7 RTK7721000B00000BR Pin Functions (7)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
H22	P4_12 / LCD0_DATA20 / LCD1_CLK / SD_CLK_0 / MMC_CLK / SPBIO10_1 / SSISCK3 / TxD1 / IRQ4	SD_CLK_0	Connected to SD card slot	CN7-18	
		LCD1_CLK	Connected to LCD1 output connector		
		SSISCK3	Connected to DAC (AK4353) 1		
J1	P7_5 / RD/WR / DV0_DATA21 / ET_TXD1 / RXD7 / SSISCK2 / TIOC1B	RD/WR	Connected to SDRAM 1 and 2	CN2-25	
		RxD7	Connected to HCI connector		
J2	P7_4 / CKE / DV0_DATA20 / ET_TXD0 / TXD7 / SSITxD1 / TIOC1A	CKE	Connected to SDRAM 1 and 2	CN2-26	
		TxD7	Connected to HCI connector		
J3	P7_3 / CAS / DV0_DATA19 / ET_TXEN / SCK7 / CTx2 / SSIRxD1 / TIOC0D	CAS	Connected to SDRAM 1 and 2	CN2-27	
		CTx2	Connected to CAN transceiver		
J4	P11_15 / SPDIF_OUT / MISO1 / IRQ1 / MMC_D7 / LCD0_CLK	LCD0_CLK	Connected to LCD0 output connector	CN2-17	
J9	Vss				
J10	Vss				
J11	Vss				
J12	Vss				
J13	Vss				
J14	Vss				
J19	Vcc				
J20	P10_9 / DV0_DATA5 / TIOC1B / ET_RXD1 / LCD0_DATA14 / VIO_D5	DV0_DATA5	Connected to DV0 input connector	CN7-5	
		LCD0_DATA14	Connected to LCD0 output connector		
		VIO_D5	Connected to CMOS camera input connector		
J21	P10_8 / DV0_DATA4 / TIOC1A / ET_RXD0 / LCD0_DATA15 / VIO_D4	DV0_DATA4	Connected to DV0 input connector	CN7-6	
		LCD0_DATA15	Connected to LCD0 output connector		
		VIO_D4	Connected to CMOS camera input connector		
J22	P4_10 / LCD0_DATA18 / LCD1_TCON5 / SD_D1_0 / MMC_D1 / SSIRxD5 / RxD0 / IRQ2	SD_D1_0	Connected to SD card slot	CN7-16	
		LCD1_TCON5	Connected to LCD1 output connector		
K1	P7_9 / A1 / SSIWS3 / ET_RXD0 / CTx0 / TIOC3B / IRQ0	A1	Address bus	CN3-30	
K2	P7_7 / WE1/DQMLU / DV0_DATA23 / ET_TXD3 / RTS7 / SSIDATA2 / TIOC2B	WE1/DQMLU	Connected to SDRAM 1 and 2	CN2-23	
		RTS7	Connected to HCI connector		
K3	P7_6 / WE0/DQMLL / DV0_DATA22 / ET_TXD2 / CTS7 / SSIWS2 / TIOC2A	WE0/DQMLL	Connected to SDRAM 1 and 2	CN2-24	
		CTS7	Connected to HCI connector		
K4	P7_8 / RD / SSISCK3 / CRx0 / TIOC3A / IRQ1	RD	Connected to NOR flash memory 1 and 2	CN2-22	
		P7_8	Connected to HCI connector		
K9	Vss				
K10	Vss				
K11	Vss				
K12	Vss				
K13	Vss				
K14	Vss				
K19	Vcc				

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Table 2.2.8 RTK7721000B00000BR Pin Functions (8)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
K20	P4_8 / LCD0_DATA16 / LCD1_TCON3 / SD_CD_0 / MMC_CD / SSISCK5 / CTx2 / SCK0 / IRQ0	SD_CD_0	Connected to SD card slot	CN7-14	
		LCD1_TCON3	Connected to LCD1 output connector		
K21	P4_9 / LCD0_DATA17 / LCD1_TCON4 / SD_WP_0 / SSIWS5 / CRx2 / TxD0 / IRQ1	SD_WP_0	Connected to SD card slot	CN7-13	
		LCD1_TCON4	Connected to LCD1 output connector		
K22	P2_1 / D17 / ET_TXER / DV0_DATA1 / SPBIO10_1 / MLB_DAT / TIOC2A / VIO_D1 / LCD0_DATA17	ET_TXER	Connected to Ethernet PHY	-	SW2-1:ON
		MLB_DAT	Connected to MOST I/F connector	CN7-23	SW2-1:OFF
L1	P11_5 / DV0_DATA17 / SD_WP_0 / SSIWS4 / LCD0_DATA2	DV0_DATA17	Connected to DV0 input connector	CN2-13	
		SSIWS4	Connected to DAC (AK4353) 2		
		LCD0_DATA2	Connected to LCD0 output connector		
L2	P7_11 / A3 / SSITxD3 / ET_RXD2 / CRx1 / TIOC3D / IRQ3	A3	Address bus	CN3-28	
L3	P7_10 / A2 / SSIRxD3 / ET_RXD1 / CTx1 / TIOC3C / IRQ2	A2	Address bus	CN3-29	
L4	P11_4 / DV0_DATA16 / SD_CD_0 / SSISCK4 / MMC_CD / LCD0_DATA3	DV0_DATA16	Connected to DV0 input connector	CN2-14	
		SSISCK4	Connected to DAC (AK4353) 2		
		LCD0_DATA3	Connected to LCD0 output connector		
L9	Vss				
L10	Vss				
L11	Vss				
L12	Vss				
L13	Vss				
L14	Vss				
L19	PVcc				
L20	P4_7 / LCD0_DATA15 / MISO1 / TIOC4D / PWM2H / SSITxD0 / DV0_DATA15	SSITxD0	Connected to audio CODEC (WM8978)	-	SW2-2:ON
		P4_7		CN6-29	SW2-2:OFF
L21	P2_0 / D16 / ET_TXCLK / DV0_DATA0 / SPBIO00_1 / MLB_CLK / IRQ5 / VIO_D0 / LCD0_DATA16	ET_TXCLK	Connected to Ethernet PHY	-	SW2-1:ON
		MLB_CLK	Connected to MOST I/F connector	CN7-24	SW2-1:OFF
L22	P4_6 / LCD0_DATA14 / MOSI1 / TIOC4C / PWM2G / SSIRxD0 / DV0_DATA14	SSIRxD0	Connected to audio CODEC (WM8978)	-	SW2-2:ON
		P4_6	NC	CN6-30	SW2-2:OFF
M1	P7_12 / A4 / SSISCK4 / ET_RXD3 / TIOC4A / IRQ4	A4	Address bus	CN3-27	
M2	P11_6 / DV0_DATA18 / SD_D1_0 / SSIDATA4 / MMC_D1 / LCD0_DATA1	DV0_DATA18	Connected to DV0 input connector	CN2-12	
		SSIDATA4	Connected to DAC (AK4353) 2		
		LCD0_DATA1	Connected to LCD0 output connector		
M3	P11_7 / DV0_DATA19 / SD_D0_0 / CTS5 / MMC_D0 / LCD0_DATA0	DV0_DATA19	Connected to DV0 input connector	CN2-11	
		LCD0_DATA0	Connected to LCD0 output connector		
M4	Vcc				
M9	Vss				
M10	Vss				
M11	Vss				

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Table 2.2.9 RTK7721000B00000BR Pin Functions (9)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
M12	Vss				
M13	Vss				
M14	Vss				
M19	PVcc				
M20	P4_5 / LCD0_DATA13 / SSL10 / TIOC4B / PWM2F / SSIWS0 / DV0_DATA13	SSIWS0	Connected to audio CODEC (WM8978)	-	SW2-2:ON
		P4_5	NC	CN6-27	SW2-2:OFF
M21	P4_4 / LCD0_DATA12 / RSPCK1 / TIOC4A / PWM2E / SSISCK0 / DV0_DATA12	SSISCK0	Connected to audio CODEC (WM8978)	-	SW2-2:ON
		P4_4	NC	CN6-28	SW2-2:OFF
M22	P10_7 / DV0_DATA3 / TIOC0D / PWM2H / ET_TXD3 / LCD0_DATA16 / VIO_D3	DV0_DATA3	Connected to DV0 input connector	CN6-23	
		LCD0_DATA16	Connected to LCD0 output connector		
		VIO_D3	Connected to CMOS camera input connector		
N1	P7_13 / A5 / SSIWS4 / ET_MDIO / TIOC4B / IRQ5	A5	Address bus	CN3-26	
N2	P7_14 / A6 / SSIDATA4 / ET_CRS / TIOC4C / IRQ6	A6	Address bus	CN3-25	
N3	P7_15 / A7 / RSPCK0 / ET_RXCLK / CTS5 / SCI_TXD0 / TIOC4D	A7	Address bus	CN3-24	
N4	PVcc				
N9	Vss				
N10	Vss				
N11	Vss				
N12	Vss				
N13	Vss				
N14	Vss				
N19	P10_4 / DV0_DATA0 / TIOC0A / PWM2E / ET_TXD0 / LCD0_DATA19 / VIO_D0	DV0_DATA0	Connected to DV0 input connector	CN6-22	
		LCD0_DATA19	Connected to LCD0 output connector		
		VIO_D0	Connected to CMOS camera input connector		
N20	P10_5 / DV0_DATA1 / TIOC0B / PWM2F / ET_TXD1 / LCD0_DATA18 / VIO_D1	DV0_DATA1	Connected to DV0 input connector	CN6-21	
		LCD0_DATA18	Connected to LCD0 output connector		
		VIO_D1	Connected to CMOS camera input connector		
N21	P10_6 / DV0_DATA2 / TIOC0C / PWM2G / ET_TXD2 / LCD0_DATA17 / VIO_D2	DV0_DATA2	Connected to DV0 input connector	CN6-24	
		LCD0_DATA17	Connected to LCD0 output connector		
		VIO_D2	Connected to CMOS camera input connector		
N22	P4_3 / LCD0_DATA11 / TIOC0D / FWE / CTx3 / Rx D2 / MISO4 / MMC_D7	FWE	Connected to NAND flash memory	CN6-17	
		MMC_D7	Connected to MMC card slot		
		MISO4	Connected to audio CODEC (WM8978)		
			Connected to CD deck connector		
P1	P8_0 / A8 / SSL00 / ET_RXER / SCK5 / SCI_SCK0	A8	Address bus	CN3-23	
P2	P8_1 / A9 / MOSI0 / ET_RXDV / TXD5 / SCI_RXD0	A9	Address bus	CN3-21	
P3	P8_2 / A10 / MISO0 / RXD5 / IRQ0	A10	Address bus	CN3-20	
P4	PVcc				
P9	Vss				
P10	Vss				
P11	Vss				
P12	Vss				
P13	Vss				

: 3.3V system power supply,
 : 1.18V system power supply,
 : GND,
 Letters in Red indicate CPU board setting.

Table 2.2.10 RTK7721000B00000BR Pin Functions (10)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
P14	Vss				
P19	Vss				
P20	P4_0 / LCD0_DATA8 / TIOC0A / FRE / RSPCK4 / MMC_D4	FRE	Connected to NAND flash memory	CN6-16	
		MMC_D4	Connected to MMC card slot		
		RSPCK4	Connected to audio CODEC (WM8978)		
			Connected to CD deck connector		
P21	P4_2 / LCD0_DATA10 / TIOC0C / FALE / CRx3 / TxD2 / MOSI4 / MMC_D6	FALE	Connected to NAND flash memory	CN6-18	
		MMC_D6	Connected to MMC card slot		
		MOSI4	Connected to audio CODEC (WM8978)		
			Connected to CD deck connector		
P22	P4_1 / LCD0_DATA9 / TIOC0B / FCLE / SCK2 / SSL40 / MMC_D5	FCLE	Connected to NAND flash memory	CN6-15	JP10:Open
		MMC_D5	Connected to MMC card slot		
		SSL40	Connected to audio CODEC (WM8978)		JP10:Short
R1	P8_3 / A11 / DV1_DATA0 / RSPCK2 / RTS5 / IRQ1 / SCK2	A11	Address bus	CN3-19	
R2	P8_4 / A12 / DV1_DATA1 / SSL20 / IERxD / RxD2	A12	Address bus	CN3-18	
R3	P8_5 / A13 / DV1_DATA2 / MOSI2	A13	Address bus	CN3-17	
R4	Vcc				
R19	Vcc				
R20	P3_15 / LCD0_DATA7 / NAF7 / TRACECTL / SD_D2_1 / MMC_D2	NAF7	Connected to NAND flash memory	CN6-11	
		SD_D2_1	Connected to MMC card slot		
		MMC_D2			
R21	P3_14 / LCD0_DATA6 / NAF6 / TRACECLK / SD_D3_1 / MMC_D3	NAF6	Connected to NAND flash memory	CN6-12	
		SD_D3_1	Connected to MMC card slot		
		MMC_D3			
		TRACECLK	Connected to UDI connector		
R22	P3_13 / LCD0_DATA5 / NAF5 / AUDIO_XOUT / SD_CMD_1 / MMC_CMD	NAF5	Connected to NAND flash memory	CN6-9	
		SD_CMD_1	Connected to MMC card slot		
		MMC_CMD			
T1	P11_8 / DV0_DATA20 / SD_CLK_0 / RTS5 / MMC_CLK / LCD0_TCON6	DV0_DATA20	Connected to DV0 input connector	CN2-8	
		LCD0_TCON6	Connected to LCD0 output connector		
T2	P11_9 / DV0_DATA21 / SD_CMD_0 / SCK5 / MMC_CMD / LCD0_TCON5	DV0_DATA21	Connected to DV0 input connector	CN2-7	
		LCD0_TCON5	Connected to LCD0 output connector		
T3	P11_10 / DV0_DATA22 / SD_D3_0 / TxD5 / MMC_D3 / LCD0_TCON4	DV0_DATA22	Connected to DV0 input connector	CN2-6	
		LCD0_TCON4	Connected to LCD0 output connector		
T4	Vcc				
T19	Vcc				
T20	P3_10 / LCD0_DATA2 / NAF2 / TRACEDATA2 / TIOC4C / SD_D1_1 / MMC_D1	NAF2	Connected to NAND flash memory	CN6-4	
		SD_D1_1	Connected to MMC card slot		
		MMC_D1			
		TRACEDATA2	Connected to UDI connector		
T21	P3_11 / LCD0_DATA3 / NAF3 / TRACEDATA3 / TIOC4D / SD_D0_1 / MMC_D	NAF3	Connected to NAND flash memory	CN6-3	
		SD_D0_1	Connected to MMC card slot		
		MMC_D0			
		TRACEDATA3	Connected to UDI connector		

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 : 1.18V system power supply,
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Table 2.2.11 RTK7721000B00000BR Pin Functions (11)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
T22	P3_12 / LCD0_DATA4 / NAF4 / SD_CLK_1 / MMC_CLK	NAF4	Connected to NAND flash memory	CN6-10	
		SD_CLK_1	Connected to MMC card slot		
		MMC_CLK			
U1	Vss				
U2	P8_6 / A14 / DV1_DATA3 / MISO2 / IETxD / TxD2	A14	Address bus	CN3-16	
U3	P11_11 / DV0_DATA23 / SD_D2_0 / Rx D5 / MMC_D2 / LCD0_TCON3	DV0_DATA23	Connected to DV0 input connector	CN2-5	
		LCD0_TCON3	Connected to LCD0 output connector		
U4	P8_7 / A15 / DV1_DATA4 / AUDIO_XOUT / IRQ5 / ET_COL	A15	Address bus	CN3-15	
U19	Vcc				
U20	JP0_1 / TDO	TD0	Test data output	-	
U21	TCK		Test clock	-	
U22	Vss				
V1	CKIO		Connected to SDRAM 1 and 2	CN2-2	
V2	P8_8 / A16 / DV1_DATA5 / SPBIO00_1 / SPDIF_IN / TIOC1A / PWM1A / Tx D3 / SSISCK5	A16	Address bus	CN3-14	JP2:1-2
		SPDIF_IN	Connected to TOSLINK connector		JP2:2-3
V3	P8_9 / A17 / DV1_DATA6 / SPBIO10_1 / SPDIF_OUT / TIOC1B / PWM1B / Rx D3 / SSIWS5	A17	Address bus	CN3-12	
		SPDIF_OUT	Connected to TOSLINK connector		
V4	P8_13 / A21 / SPBSSL_1 / TIOC3D / TXD5 / PWM1F / SGOUT_3 / SSIWS4	A21	Address bus	CN3-8	JP8:Open
		SPBSSL_1	Connected to serial flash memory 3		JP8:Short
V19	P3_8 / LCD0_DATA0 / NAF0 / TRACEDATA0 / TIOC4A / SD_CD_1 / MMC_CD	NAF0	Connected to NAND flash memory	CN6-2	
		SD_CD_1	Connected to MMC card slot		
		MMC_CD			
		TRACEDATA0	Connected to UDI connector		
V20	TRST#		Initialization signal input pin	-	
V21	JP0_0 / TDI	TDI	Test data input	-	
V22	TMS		Test mode select	-	
W1	Vss				
W2	P8_10 / A18 / DV1_DATA7 / SPBIO20_1 / TIOC3A / CTx4 / PWM1C / SGOUT_0 / SSITxD5	A18	Address bus	CN3-11	
		SPBIO20_1	Connected to serial flash memory 3		
W3	P8_11 / A19 / SPBIO30_1 / TIOC3B / Rx D5 / PWM1D / SGOUT_1 / DV0_CLK	A19	Address bus	CN3-10	
		SPBIO30_1	Connected to serial flash memory 3		
W4	PVcc				
W5	PVcc				
W6	PVcc				
W7	Vss				
W8	Vss				
W9	Vcc				
W10	Vcc				
W11	Vss				
W12	PVcc				
W13	PVcc				
W14	PLL Vcc				

: 3.3V system power supply,
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Table 2.2.12 RTK7721000B00000BR Pin Functions (12)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
W15	Vss				
W16	Vss				
W17	AVss			CN5-13, 14	
W18	AVcc			CN5-9, 10	
W19	PVcc				
W20	P3_9 / LCD0_DATA1 / NAF1 / TRACEDATA1 / TI0C4B / SD_WP_1 / IRQ6	NAF1	Connected to NAND flash memory	CN6-1	
		SD_WP_1	Connected to MMC card slot		
		TRACEDATA1	Connected to UDI connector		
W21	AUDIO_X2		Open	-	
W22	AUDIO_X1		Connects audio external clock	-	22.5792MHz
Y1	P8_12 / A20 / SPBCLK_1 / TI0C3C / SCK5 / PWM1E / SGOUT_2 / SSISCK4	A20	Address bus	CN3-9	
		SPBCLK_1	Connected to serial flash memory 3		
Y2	P8_14 / A22 / SPBIO01_0 / SPBIO00_1 / TI0C2A / RSPCK2 / PWM1G / TxD4 / SSIDATA4	A22	Address bus	CN3-7	
		SPBIO01_0	Connected to serial flash memory 3		
Y3	PVcc				
Y4	P3_7 / LCD0_TCON6 / SSITxD1 / LCD1_EXTCLK / SCI_CTS0/RTS0 / TI0C3D / CS1 / WDTOVF	LCD1_EXTCLK	Connects external clock for LCD panel	CN4-13	X9 (optional) JP6:1-2
		CS1	Connected to NOR flash memory 2		JP6:2-3
Y5	P3_4 / LCD0_TCON3 / ET_RXCLK / SSISCK1 / AUDIO_XOUT2 / SCI_SCK0 / TI0C3A / SCK3	ET_RXCLK	Connected to Ethernet PHY	CN4-12	SW2-1:ON
		SSISCK1	Connected to CD deck connector		SW2-1:OFF SW14-7:OFF
		SCI_SCK0	Connected to SIM card slot		SW2-1:OFF
		SCK3	Connected to UART connector		SW14-7:ON
Y6	P10_2 / DV0_HSYNC / TCLKC / PWM2C / ET_TXEN / LCD0_DATA21 / VIO_HD	DV0_HSYNC	Connected to DV0 input connector	CN4-18	
		LCD0_DATA21	Connected to LCD0 output connector		
		VIO_HD	Connected to CMOS camera input connector		
Y7	P3_2 / LCD0_TCON1 / ET_TXEN / RxD2 / SCI_RXD1 / TEND0 / PWM2C / MOSI3	RxD2	Connected to D-sub 9-pin connector via RS-232C transceiver	CN4-8	JP12:1-2
			Connected to USB-miniB connector via USB serial conversion IC		JP12:2-3
Y8	RES#		Connected to reset input switch	CN4-2	
Y9	NMI		Connected to non-maskable interrupt switch	CN4-1	
Y10	Vss				
Y11	VBUSIN1		USB channel 1 VBUS input	-	JP11
Y12	VBUSIN0		USB channel 0 VBUS input	CN5-17, 18	JP9
Y13	USBAVcc		Transceiver unit analog core power supply		
Y14	Vss				
Y15	P0_0 / MD_BOOT0	MD_BOOT0	Connected to DIPSW as a boot mode input	-	SW1-1
Y16	P0_1 / MD_BOOT1	MD_BOOT1	Connected to DIPSW as a boot mode input	-	SW1-2
Y17	P1_10 / AN2 / IRQ4 / TCLKB	AN2	Connected to key input switch	CN5-16	
Y18	P1_13 / AN5 / DV0_HSYNC / WAIT	P1_13	Connected to CD deck connector (FLAG6)	CN5-11	
Y19	P1_15 / AN7	P1_15	Connected to Ethernet PHY (INT / GPIO4)	CN5-7	
Y20	PVcc				
Y21	VIDEO_X2		Open	-	
Y22	VIDEO_X1		Connects external clock for video decoder	-	27MHz
AA1	P8_15 / A23 / SPBIO11_0 / SPBIO10_1 / TI0C2B / SSL20 / PWM1H / RxD4	A23	Address bus	CN3-6	
		SPBIO11_0	Connected to serial flash memory 3		

: 3.3V system power supply,
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Table 2.2.13 RTK7721000B00000BR Pin Functions (13)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
AA2	PVcc				
AA3	P9_1 / A25 / SPBIO31_0 / CRx0 / IRQ0 / MISO2	A25	Address bus	CN3-3	
AA4	P3_5 / LCD0_TCON4 / ET_RXER / SSIWS1 / AUDIO_XOUT3 / SCI_TXD0 / TIOC3B / TxD3	ET_RXER	Connected to Ethernet PHY	-	SW2-1:ON
		SSIWS1	Connected to CD deck connector	CN4-11	SW2-1:OFF SW14-7:OFF
		SCI_TXD0	Connected to SIM card slot		SW2-1:OFF SW14-7:ON JP1:Short
			Connected to IrDA module		SW2-1:OFF SW14-7:ON JP1:Open
		TxD3	Connected to UART connector		SW2-1:OFF SW14-7:ON JP1:Open
AA5	P10_1 / DV0_VSYNC / TCLKB / PWM2B / ET_TXER / LCD0_DATA22 / VIO_VD	DV0_VSYNC	Connected to DV0 input connector	CN4-19	
		LCD0_DATA22	Connected to LCD0 output connector		
		VIO_VD	Connected to CMOS camera input connector		
AA6	P3_3 / LCD0_TCON2 / ET_MDIO / IRQ4 / BS / SCI_CTS1 / RTS1 / DACK0 / PWM2D / MISO3	ET_MDIO	Connected to Ethernet PHY	-	SW2-1:ON
		P3_3	Connected to CD deck connector (SSL40)	CN4-7	SW2-1:OFF SW14-7:OFF
			Connected to SIM card slot (reset)		SW2-1:OFF SW14-7:ON
AA7	P3_1 / LCD0_TCON0 / ET_TXER / IRQ6 / TxD2 / SCI_TXD1 / AUDIO_CLK / PWM2B / SSL30	IRQ6	Connected to interrupt switch	-	JP3:1-2
			Connected to CD deck connector	CN4-5	JP3:2-3
		AUDIO_CLK	Connected to HCI connector		
AA8	RTC_X2		Connects RTC resonator	-	32.768KHz
AA9	P0_5 / RTC_X4	RTC_X4	Open	-	
AA10	Vss				
AA11	DM_1		USB channel 1 differential signal D- data	-	
AA12	DP_0		USB channel 0 differential signal D+ data	-	
AA13	REFRIN		Reference input	-	5.6k Ω ±1%
AA14	Vss				
AA15	USB_X2		Open	-	
AA16	XTAL		Open	-	
AA17	P1_8 / AN0 / IRQ2 / DREQ0 / VIO_D14 / DV0_DATA14	AN0	Connected to key input switch	CN5-20	
AA18	P1_11 / AN3 / IRQ5 / TCLKD	AN3	Connected to key input switch	CN5-15	
AA19	P1_14 / AN6 / ET_COL	ET_COL	Connected to Ethernet PHY	CN5-8	
AA20	AVcc			CN5-9, 10	
AA21	PVcc				
AA22	BSCANP		Connected to DIPSW as a pin for boundary scan mode setting	-	SW2-3
AB1	PVcc				
AB2	P9_0 / A24 / SPBIO21_0 / CTx0 / TCLKC / MOSI2	A24	Address bus	CN3-5	

: 3.3V system power supply,
 : 1.18V system power supply,
 : GND,
 Letters in Red indicate CPU board setting.

Table 2.2.14 RTK7721000B00000BR Pin Functions (14)

Pin No.	Pin Name	Function	Description	Expansion Connector	Remarks
AB3	P3_6 / LCD0_TCON5 / ET_RXDV / SSIRxD1 / SCI_RXD0 / TIOC3C / RxD3	ET_RXDV	Connected to Ethernet PHY	-	SW2-1:ON
		SSIRxD1	Connected to CD deck connector	CN4-14	SW2-1:OFF SW14-7:OFF
		SCI_RXD0	Connected to SIM card slot		SW2-1:OFF SW14-7:ON JP1:Short JP5:Open
			Connected to IrDA module		SW2-1:OFF SW14-7:ON JP1:Open JP5:Short
		RxD3	Connected to UART connector		SW2-1:OFF SW14-7:ON JP1:Open JP5:Open
AB4	P10_0 / DV0_CLK / TCLKA / PWM2A / ET_TXCLK / LCD0_DATA23 / VIO_CLK	DV0_CLK	Connected to DV0 input connector	CN4-20	
		LCD0_DATA23	Connected to LCD0 output connector		
		VIO_CLK	Connected to CMOS camera input connector		
AB5	P10_3 / TCLKD / PWM2D / ET_CRS / LCD0_DATA20 / VIO_FLD	LCD0_DATA20	Connected to LCD0 output connector	CN4-17	
		P10_3	Connected to CMOS camera input connector (reset control)		JP4:2-3
AB6	P3_0 / LCD0_CLK / ET_TXCLK / IRQ2 / SCK2 / SCI_SCK1 / TxD2 / PWM2A / RSPCK3	TxD2	Connected to D-sub 9-pin connector via RS-232C transceiver	CN4-6	JP13:1-2
			Connected to USB-miniB connector via USB serial conversion IC		JP13:2-3
AB7	Vss				
AB8	RTC_X1		Connects RTC resonator	-	32.768KHz
AB9	P0_4 / RTC_X3	RTC_X3	Connects RTC external clock	-	4MHz
AB10	Vss				
AB11	DP_1		USB channel 1 differential signal D+ data	-	
AB12	DM_0		USB channel 0 differential signal D- data	-	
AB13	Vss				
AB14	USBAPVcc		Transceiver unit analog pin power supply		
AB15	USB_X1		Connects USB external clock	-	48MHz
AB16	EXTAL		Connects crystal resonator as a system clock source	-	13.33MHz
AB17	Vss				
AB18	P1_9 / AN1 / IRQ3 / VIO_D15 / DV0_DATA15	AN1	Connected to key input switch	CN5-19	
AB19	P1_12 / AN4 / DV0_VSYNC / VIO_FLD	P1_12	Connected to CD deck connector (TRANS)	CN5-12	
AB20	AVss			CN5-13, 14	
AB21	AVref		ADC analog reference voltage		
AB22	Vss				

: 3.3V system power supply,
 : 1.18V system power supply,
 : GND,
 Letters in Red indicate CPU board setting.

2.2.3 RTK7721000B00000BR Module Applicability

The symbol of "Y" in the table indicates that both modules can be used in combination, and the "N" indicates that combination use is not applicable.

Table 2.2.15 lists the RTK7721000B00000BR Module Applicability.

Table 2.2.15 RTK7721000B00000BR Module Applicability

		RTK772100BC00000BR																								RTK7721000B00000BR																							
Module Name		NOR flash memory 1	NOR flash memory 2	SDRAM1	SDRAM2	Serial flash memory 1 and 2	Serial flash memory 3	NAND flash memory	EEPROM	USB	Ethernet	Video input	LCD output (LCD1_EXTCLK)	Audio CODEC	CAN1	CAN2	SD card slot	MMC card slot	LVDS output	TOSLINK	MOST	CoreSight 20	ARM JTAG 20	IRQ6 switch	Serial port	SIM card slot	IrDA	UART	IEBus	LIN	HCI	CD deck	Key input	Audio DAC1	Audio DAC2	LCD output 1 (ch0)	LCD output 2 (ch1)	LCD output (LCD0_EXTCLK)	CMOS camera input	Digital video signal input 1 (ch0)									
RTK772100BC00000BR	NOR flash memroy 1	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	NOR flash memory 2	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	SDRAM1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	SDRAM2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	Serial flash memory 1 and 2 *4	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	Serial flash memroy 3	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	NAND flash memory	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y									
	EEPROM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	USB	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	Ethernet	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	Y	Y	Y	N	Y	Y	Y									
	Video input	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	LCD output (LCD1_EXTCLK)	Y	*1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	Audio CODEC (WM8978)	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	CAN1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	CAN2	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	SD card slot (4 bits)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y								
	MMC card slot (8 bits)	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	N	Y	Y	Y	Y	Y								
	LVDS output	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y								
	TOSLINK	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	MOST	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	CoreSight 20	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	ARM JTAG 20	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	IRQ6 switch	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y								
	Serial port	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y							
RTK7721000B00000BR	SIM card slot	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	IrDA	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	UART	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	IEBus	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	N	Y	Y									
	LIN	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y									
	HCI	N	N	N	N	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	CD deck	Y	Y	Y	Y	Y	Y	N	Y	Y	N	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y								
	Key input	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	Audio DAC1 (AK4353)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y									
	Audio DAC2 (AK4353)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y										
	LCD output 1 (ch0)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	N	Y	Y									
	LCD output 2 (ch1)	Y	Y	Y	Y	N	Y	N	Y	Y	Y	N	Y	Y	Y	Y	N	Y	*3	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y									
	LCD output (LCD0_EXTCLK)	Y	Y	*2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y									
	CMOS camera input	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	N	Y									
	Digital video signal input 1 (ch0)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y									
	Digital video signal input 2 (ch1)	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	*3	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y									
Part No.		U2	U3	U4	U5	U6, U7	U8	U9	U10	J5, J8	J10	J1	X9	J4, J6	J12	J13	J11	J15	J14	U26	J3	J21	J22	SW6	J17, J19	J2	U3	J3	J4	J5	J7	J8	SW13	J6	J9	J10, J11, J15	J12~J14, J16	X1	J17	J18									

*1: P3_7 / CS1 / LCD1_EXTCLK are the common pins. These pins can be used in combination when LCD1_EXTCLK is not used.
The oscillator should be mounted to X0 on the RTK772100BC00000BR when using LCD1_EXTCLK.

*2: P5_8 / CS2 / LCD0_EXTCLK are the common pins. These pins can be used in combination when LCD0_EXTCLK is not used.
The oscillator should be mounted to X1 when using LCD0_EXTCLK.

*3: R315 to R318 or R14, R16, R17, R20, R22, R24, R26 and R29 on the RTK772100BC00000BR need to be removed.

*4: Set SPBCLK_0 less than 33.33MHz or disconnect JP6 when using the serial flash memory 1 and 2 in the RTK7721000B00000BR connected.

2.3 IEBus Interface

The R7S72100 includes a smaller digital data transmission system IEBus controller (EIBB) designed to execute data transmission between units. The RTK7721000B00000BR connects the R7S72100 IEBB pin to the 4-pin 2.5mm pitch connector via the IEBus transceiver IC.

Figure 2.3.1 shows the IEBus Interface Block Diagram. Table 2.3.1 lists the RTK772100BC00000BR JP4 Function Setting, and Table 2.3.2 lists the JP7 and JP2 Function Settings.

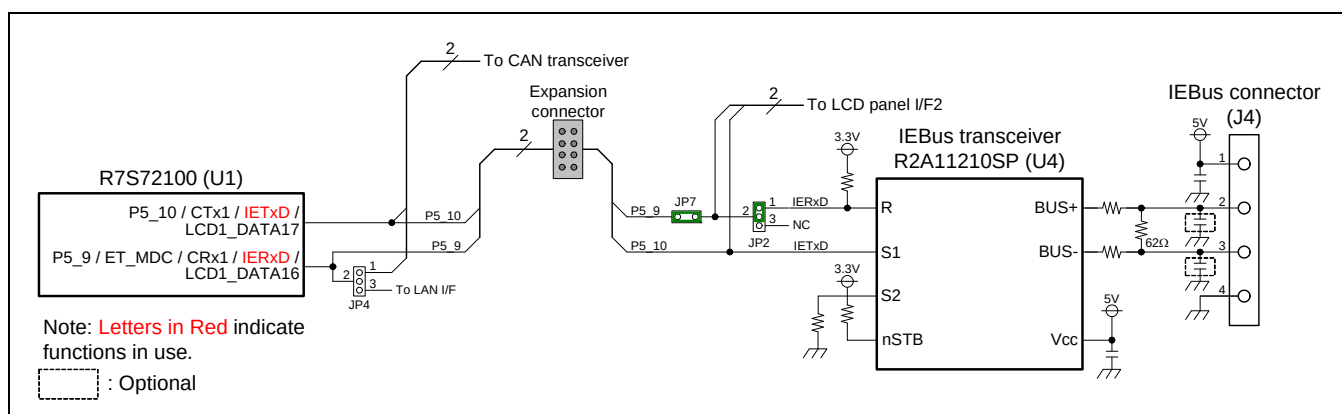


Figure 2.3.1 IEBus Interface Block Diagram

Table 2.3.1 RTK772100BC00000BR JP4 Function Setting

Jumper	1-2	2-3	None
JP4	Use P5_9 as CRx1 input pin	Use P5_9 as ET_MDC output pin (initial setting)	Use P5_9 as IERxD input pin or LCD1_DATA16 output pin

indicates setting function.

Table 2.3.2 JP7 and JP2 Function Settings

Jumper	1-2	2-3 or Open
JP7	Use P5_9 as IERxD input pin or LCD1_DATA16 output pin	Use P5_9 as ET_MDC output pin (initial setting)
JP2	Use P5_9 as IERxD input pin	Use P5_9 as LCD1_DATA16 output pin (initial setting)

indicates setting function.

2.4 LIN Interface

The R7S72100 includes a LIN/UART interface (RLIN3). The RTK7721000B00000BR connects the R7S72100 RLIN3 pin to the 3-pin 2.5mm pitch connector via the LIN transceiver IC.

Figure 2.4.1 shows the LIN Interface Block Diagram. Table2.4.1 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting, and Table2.4.2 lists the JP3 Function Setting.

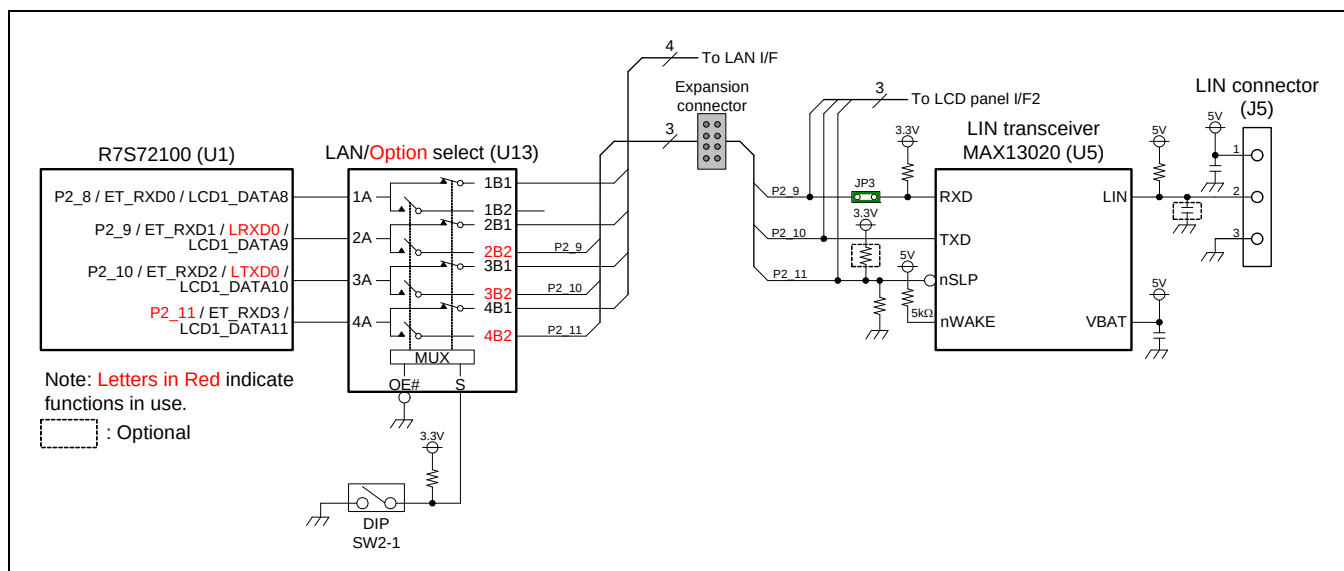


Figure 2.4.1 LIN Interface Block Diagram

Table2.4.1 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_[6:3] and P2_[11:0] as Ethernet PHY control pin (initial setting)	Use P3_[6:3] and P2_[11:0] as MOST control pin and expansion connector pin

■ indicates setting function.

Table2.4.2 JP3 Function Setting

Jumper	Short	Open
JP3	Use P2_9 as LRXD0 input pin	Use P2_9 as LCD1_DATA9 output pin (initial setting)

■ indicates setting function.

2.5 SIM Card Interface

The serial communication interface (SCI) embedded in the R7S72100 responds to the smart card (IC card) interface for the ISO/IEC7816-3 (Identification Card) as extension with asynchronous communication mode. The RTK7721000B00000BR connects the R7S72100 SCI pin to the SIM card slot.

Figure 2.5.1 shows the SIM Card Interface Block Diagram. Table2.5.1 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting, Table2.5.2 lists the SW14-7 (DIP Switch for System Setting) Function Setting, and Table2.5.3 lists the JP1 and JP5 Function Settings.

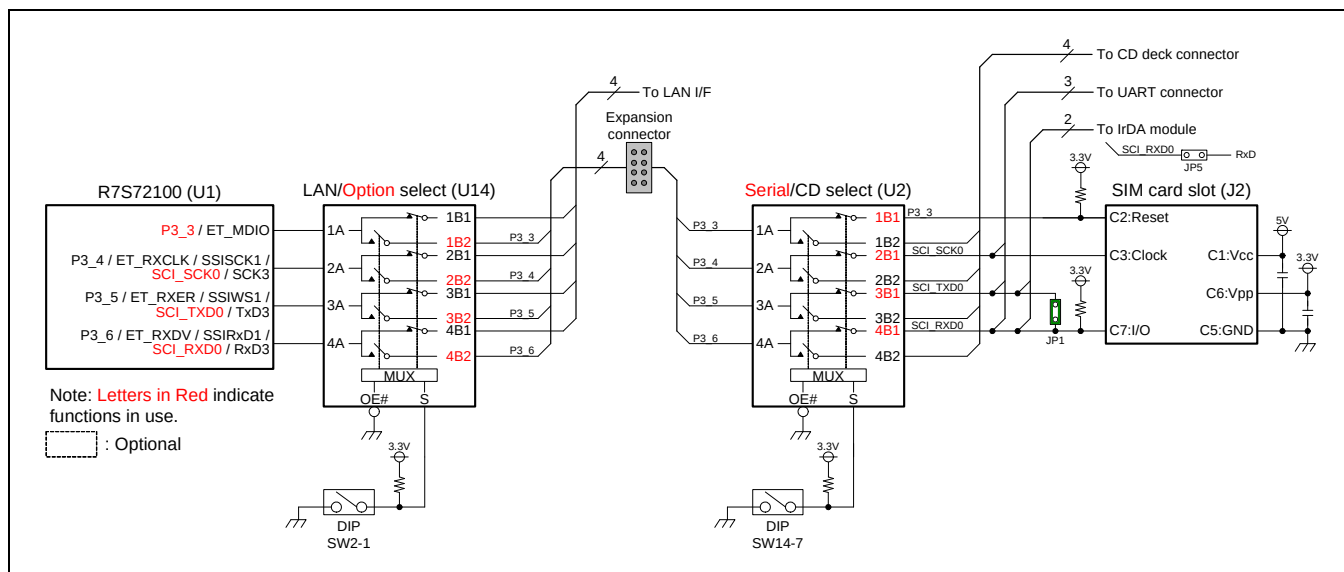


Figure 2.5.1 SIM Card Interface Block Diagram

Table2.5.1 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_[6:3] and P2_[11:0] as Ethernet PHY control pin (initial setting)	Use P3_[6:3] and P2_[11:0] as MOST control pin and expansion connector pin

■ indicates setting function.

Table2.5.2 SW14-7 (DIP Switch for System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW14-7	Use P3_[6:3] as SCI pin (initial settin)	Use P3_[6:3] as SSIF pin

■ indicates setting function.

Table2.5.3 JP1 and JP5 Function Settings

Jumper	Short	Open
JP1	Use SCI in smart card interface mode	Use SCI in serial communication interface mode (initial setting)
JP5	Connect SCI_RXD0 pin to IrDA module	Do not connect SCI_RXD0 pin to IrDA module (initial settin)

■ indicates setting function.

2.6 IrDA Module

The R7S72100 includes a serial communication interface (SCI) which transmits/receives the IrDA (infrared Data Association) communication waveform based on the IrDA standard working with the IrDA module. The RTK7721000B00000BR connects the R7S72100 SCI pin to the IrDA module.

Figure 2.6.1 shows the IrDA Module Block Diagram. Table2.6.1 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting, Table2.6.2 lists the SW14-7 (DIP Switch for System Setting) Function Setting, and Table2.6.3 lists the JP1 and JP5 Function Settings.

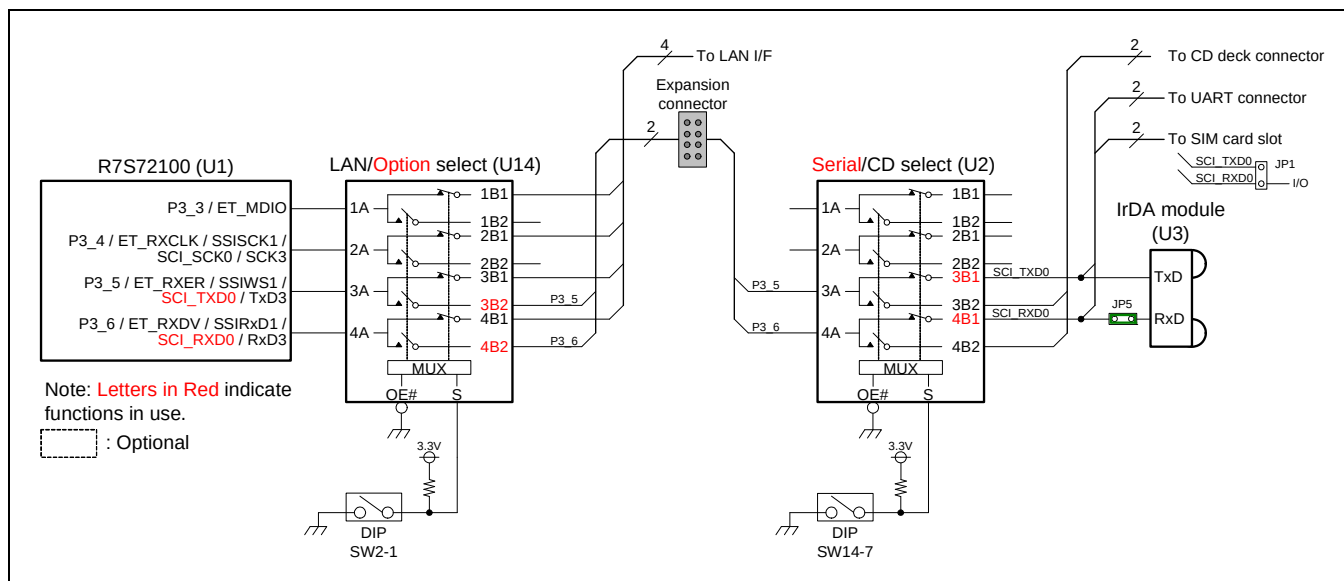


Figure 2.6.1 IrDA Module Block Diagram

Table2.6.1 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_[6:3] and P2_[11:0] as Ethernet PHY control pin (initial setting)	Use P3_[6:3] and P2_[11:0] as MOST control pin and expansion connector pin

■ indicates setting function.

Table2.6.2 SW14-7 (DIP Switch for System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW14-7	Use P3_[6:3] as SCI pin (initial setting)	Use P3_[6:3] as SSIF pin

■ indicates setting function.

Table2.6.3 JP1 and JP5 Function Settings

Jumper	Short	Open
JP1	Use SCI in smart card interface mode	Use SCI in serial communication interface mode (initial setting)
JP5	Connect SCI_RXD0 pin to IrDA module	Do not connect SCI_RXD0 pin to IrDA module (initial setting)

■ indicates setting function.

2.7 UART Interface

The R7S72100 includes a serial communication interface (SCI). The RTK7721000B00000BR connects the R7S72100 SCI pin to the 5-pin 2.5mm pitch connector.

Figure 2.7.1 shows the UART Interface Block Diagram. Table 2.7.1 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting, and Table 2.7.2 lists the SW14-7 (DIP Switch for System Setting) Function Setting.

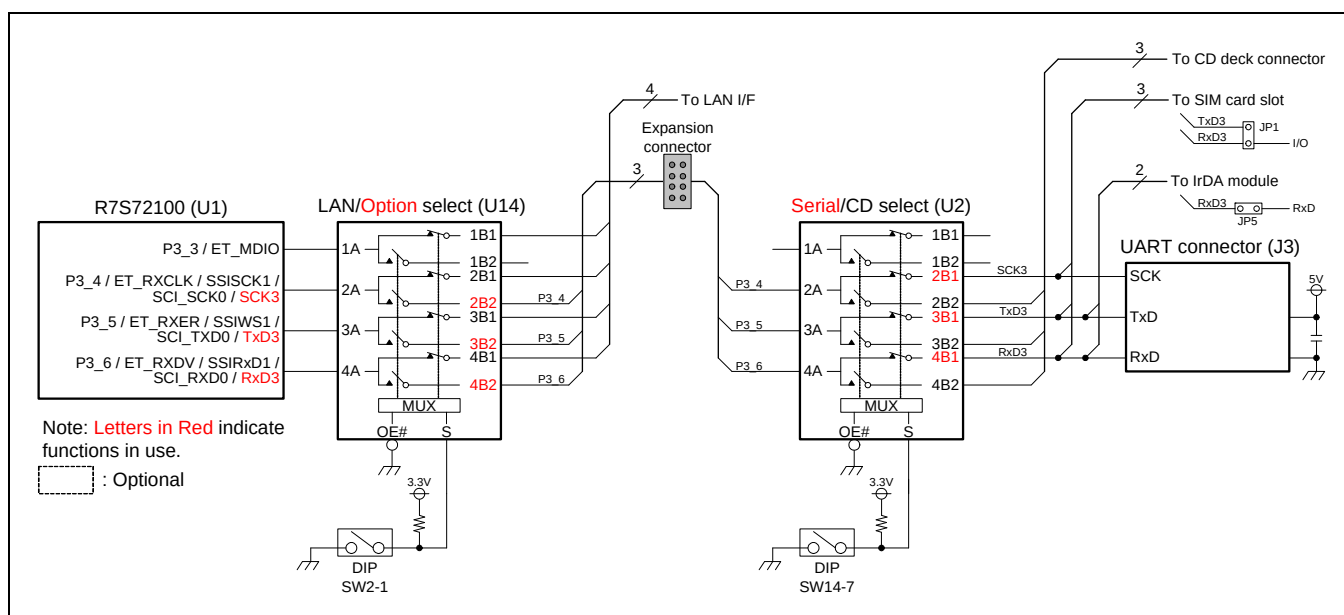


Figure 2.7.1 UART Interface Block Diagram

Table 2.7.1 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_[6:3] and P2_[11:0] as Ethernet PHY control pin (initial setting)	Use P3_[6:3] and P2_[11:0] as MOST control pin and expansion connector pin

■ indicates setting function.

Table 2.7.2 SW14-7 (DIP Switch for System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW14-7	Use P3_[6:3] as SCI pin (initial setting)	Use P3_[6:3] as SSIF pin

■ indicates setting function.

Table 2.7.3 JP1 and JP5 Function Settings

Jumper	Short	Open
JP1	Use SCI in smart card interface mode	Use SCI in serial communication interface mode (initial setting)
JP5	Connect RxD3 pin to IrDA module	Do not connect RxD3 pin to IrDA module (initial setting)

■ indicates setting function.

2.8 Audio Interface

The RTK7721000B00000BR has two audio DACs (AK4353, Asahi Kasei Microdevices) as the audio interface. The I2C bus interface (RIIC) channel 2 and the on-chip serial sound interface with FIFO (SSIF) channel 3 and 4 execute the register control for AK4353 and the output control of sound data respectively. The P4_14 pin executes the PDN control.

Figure 2.8.1 shows the Audio Interface Block Diagram.

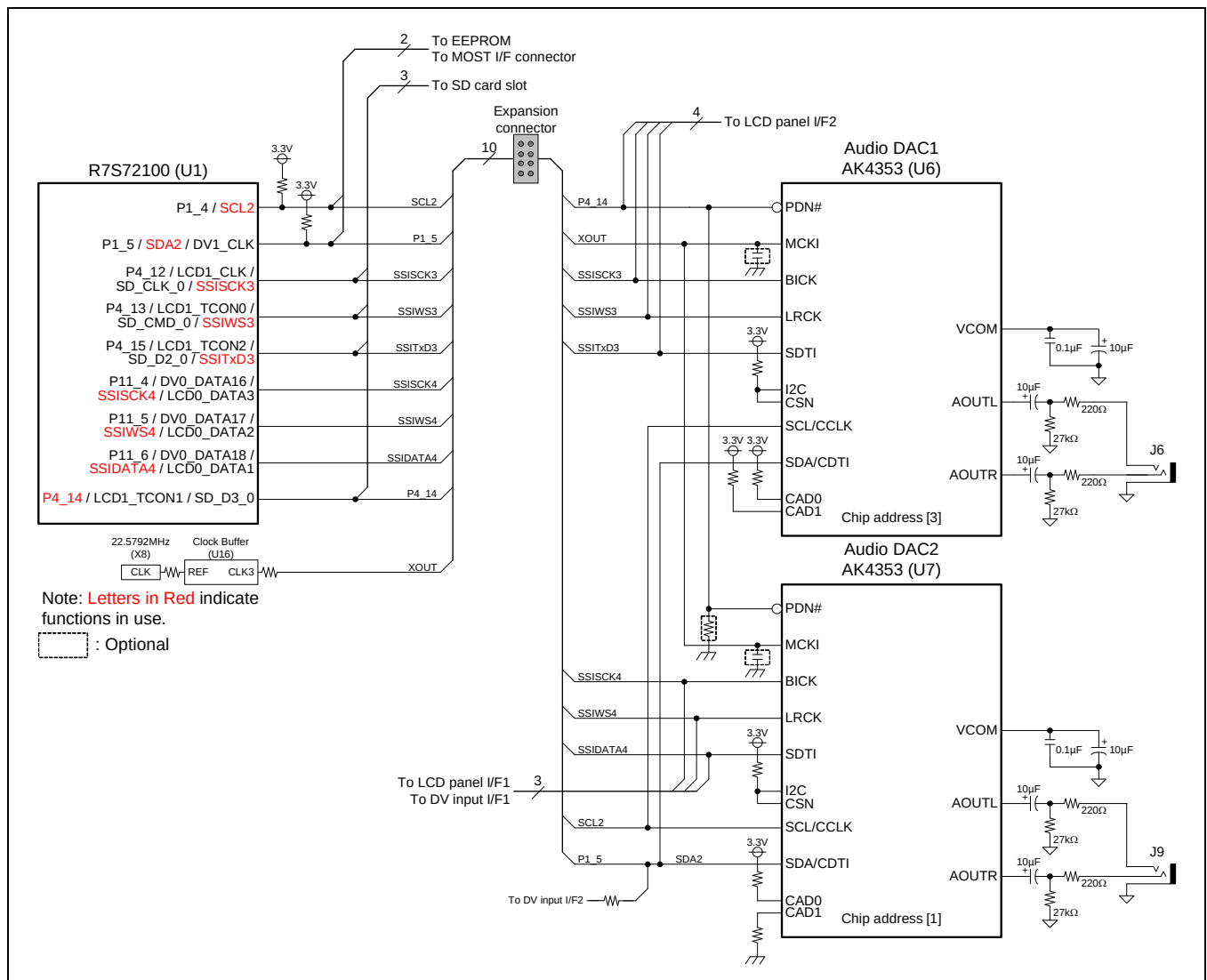


Figure 2.8.1 Audio Interface Block Diagram

2.9 CD Deck Interface

RTK7721000B00000BR has a CD deck interface connector which is controlled by the on-chip serial sound interface with FIFO (SSIF) channel 1 embedded in the R7S72100, the Renesas serial peripheral interface (RSPI) channel 4, and the general I/O ports. The RSPI pin is also used in the audio CODEC (WM8978) control on the RTK7721000B00000BR. The select signal should be output at the port P3_3 when accessing to the DC deck interface.

Figure 2.9.1 shows the CD Deck Interface Block Diagram. Table 2.9.1 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting,

Table 2.9.2 lists the SW14-7 (DIP Switch for System Setting) Function Setting, and Table 2.9.3 lists the RTK772100BC00000BR JP3 Function Setting.

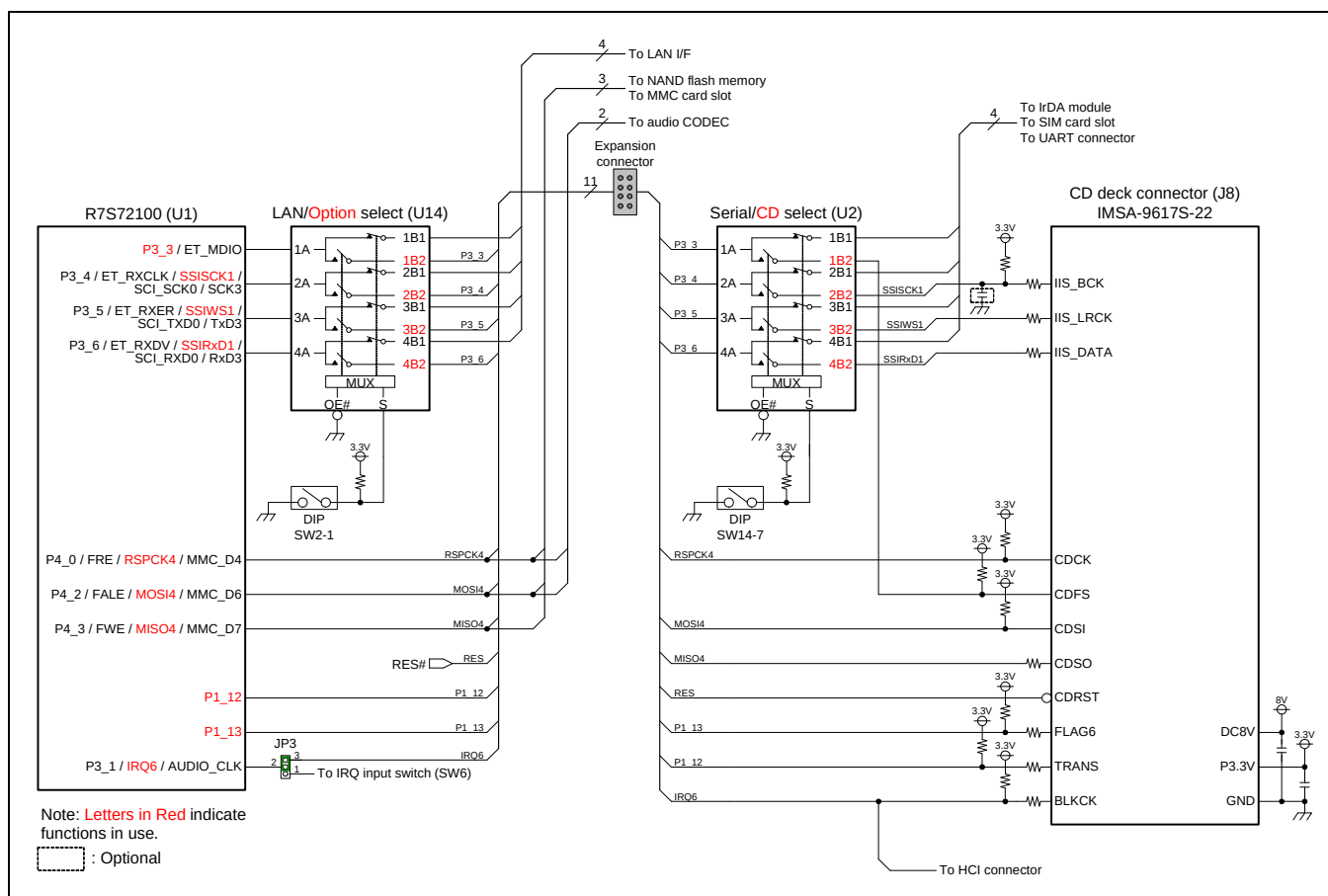


Figure 2.9.1 CD Deck Interface Block Diagram

Table 2.9.1 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_[6:3] and P2_[11:0] as Ethernet PHY control pin (initial setting)	Use P3_[6:3] and P2_[11:0] as MOST control pin and expansion connector pin

■ indicates setting function.

Table2.9.2 SW14-7 (DIP Switch for System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW14-7	Use P3_[6:3] as SCI pin (initial setting)	Use P3_[6:3] as SSIF pin

 indicates setting function.

Table2.9.3 RTK772100BC00000BR JP3 Function Setting

Jumper	1-2	2-3
JP3	Use P3_1 as IRQ6 input pin from SW6 on RTK772100BC00000BR (initial setting)	Use P3_1 as IRQ6 input pin from CD deck interface

 indicates setting function.

2.10 HCI Module Interface

The RTK7721000B00000BR has a HCI module interface connector which is connected with the R7S72100 on-chip serial communication interface with FIFO (SCIF) channel 7, on-chip serial sound interface with FIFO (SSIF) channel 5, and the I2C bus interface (RIIC) channel 0.

Figure 2.10.1 shows the HCI Module Interface Block Diagram. Table2.10.1 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting, and Table2.10.2 lists the RTK772100BC00000BR JP3 Function Setting.

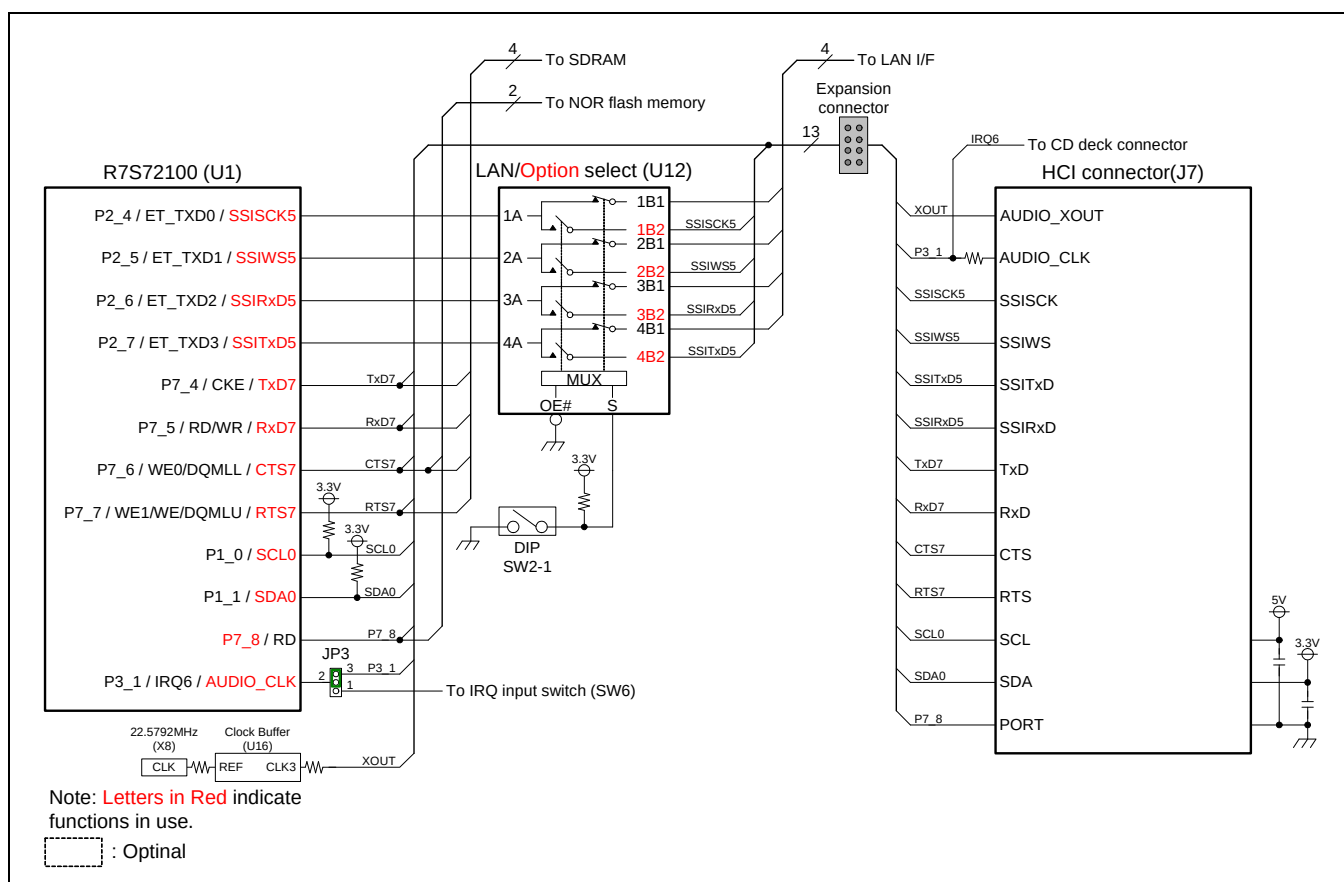


Figure 2.10.1 HCI Module Interface Block Diagram

Table2.10.1 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_1[6:3] and P2_1[11:0] as Ethernet PHY control pin (initial setting)	Use P3_1[6:3] and P2_1[11:0] as MOST control pin and expansion connector pin

■ indicates setting function.

Table2.10.2 RTK772100BC00000BR JP3 Function Setting

Jumper	1-2	2-3
JP3	Use P3_1 as IRQ6 input pin from SW6 on RTK772100BC00000BR (initial setting)	Use P3_1 as AUDIO_CLK input pin from HCI module interface

■ indicates setting function.

2.11 LCD Panel Output Interface

The RTK7721000B00000BR has 5 connectors with 3 types for the LCD panel connection. The video display controller 5 (VDC5) embedded in the R7S72100 controls the LCD panel.

An oscillator should be mounted to X9 on the RTK772100BC00000BR when using P3_7 as the LCD1_EXTCLK input pin, and to X1 when using P5_8 as the LCD0_EXTCLK pin.

The LVDS termination resistor (R315 to R318) or RL0 to RL7 (R14, R16, R17, R20, R22, R24, R26 and R29) on the RTK772100BC00000BR should be removed because the signals from LCD1_DATA0 to LCD1_DATA7 may be affected when the LCD panel output interface is used.

Table2.11.1 lists the RTK772100BC00000BR JP6 Function Setting. Figure 2.11.1 and Figure 2.11.2 show the LCD Panel Output Interface Block Diagram. Table2.11.2 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting, Table2.11.3 lists the RTK772100BC00000BR JP4 Function Setting, and Table2.11.4 lists the JP6, JP7, JP2 and JP3 Function Settings.

Table2.11.1 RTK772100BC00000BR JP6 Function Setting

Jumper	1-2	2-3
JP6	Use P3_7 as LCD1_EXTCLK input pin	Use P3_7 as CS1 output pin (initial setting)

indicates setting function.

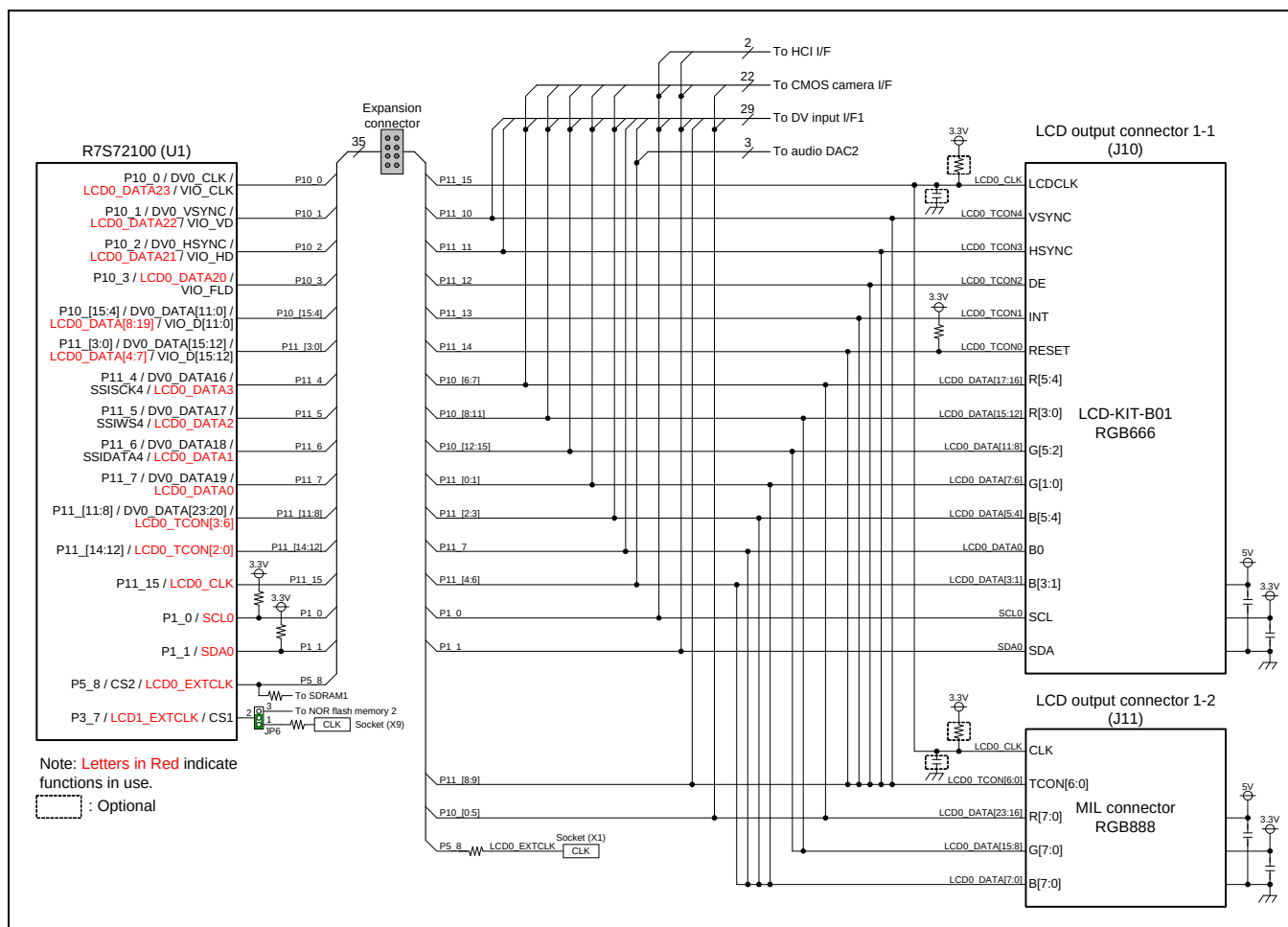


Figure 2.11.1 LCD Panel Output Interface (ch0) Block Diagram

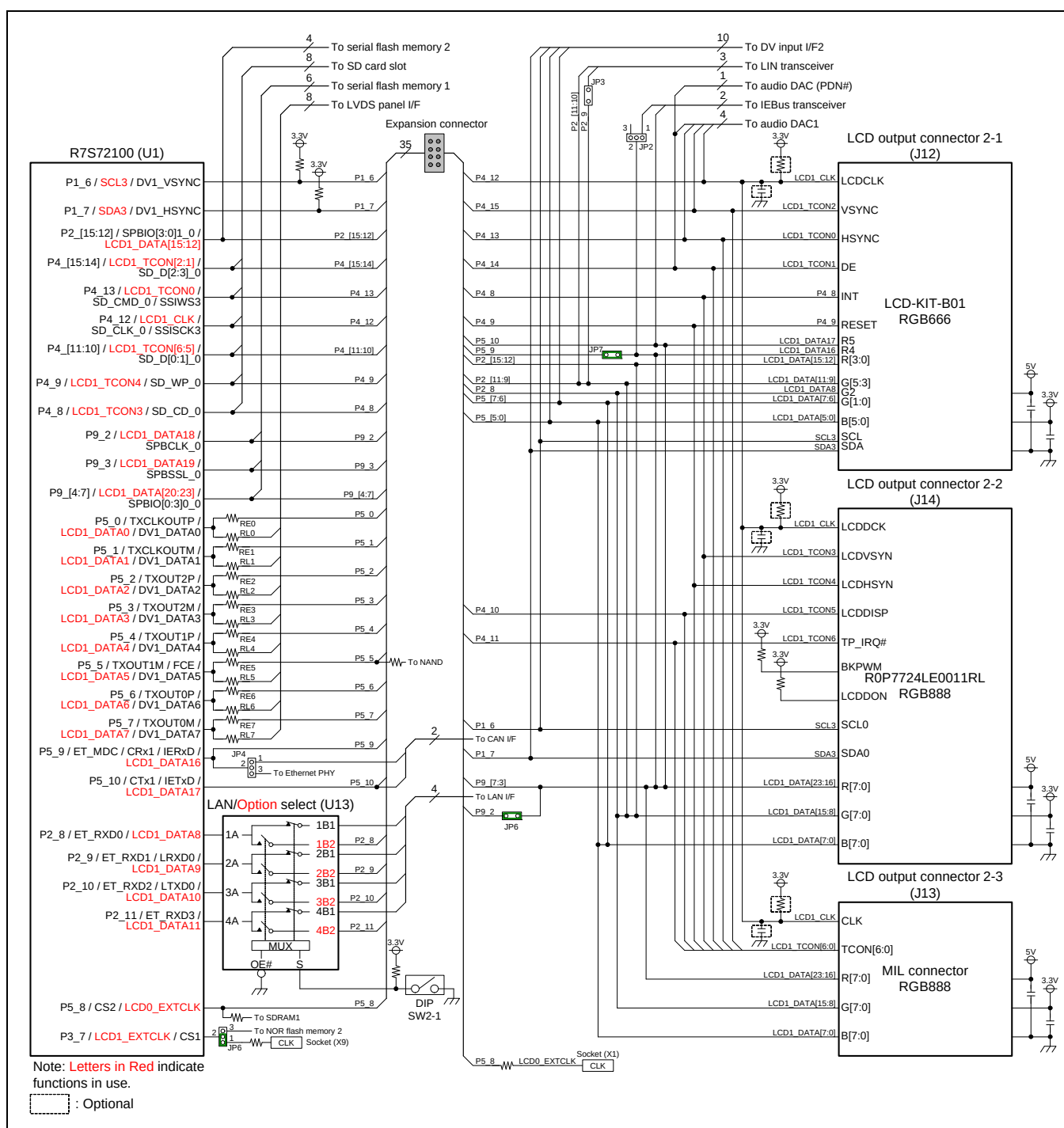


Figure 2.11.2 LCD Panel Output Interface (ch1) Block Diagram

Table 2.11.2 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_[6:3] and P2_[11:0] as Ethernet PHY control pin (initial setting)	Use P3_[6:3] and P2_[11:0] as MOST control pin and expansion connector pin

■ indicates setting function.

Table2.11.3 RTK772100BC00000BR JP4 Function Setting

Jumper	1-2	2-3	None
JP4	Use P5_9 as CRx1 input pin	Use P5_9 as ET_MDC output pin (initial setting)	Use P5_9 as IERxD input pin or LCD1_DATA16 output pin

■ indicates setting function.

Table2.11.4 JP6, JP7, JP2 and JP3 Function Settings

Jumper	1-2	2-3 or Open
JP6	Use P9_2 as LCD1_DATA18 output pin	Use P9_2 as SPBCLK_0 output pin (initial setting)
JP7	Use P5_9 as IERxD input pin or LCD1_DATA16 output pin	Use P5_9 as ET_MDC output pin (initial setting)
JP2	Use P5_9 as IERxD input pin	Use P5_9 as LCD1_DATA16 output pin (initial setting)
JP3	Use P2_9 as LRxD0 input pin	Use P2_9 as LCD1_DATA9 output pin (initial setting)

■ indicates setting function.

2.12 Analog RGB Output Interface

The RTK7721000B00000BR includes video DACs and converts the LCD panel control signal to the analog RGB. The signal of the converted analog RGB is output from the D-sub 15-pin connector.

The oscillator should be mounted to X9 the RTK772100BC00000BR when using P3_7 as the LCD1_EXTCLK input pin, and to X1 when using P5_8 as the LCD0_EXTCLK pin.

The LVDS termination resistors (R315 to R318) or RL0 o RL7 (R14, R16, R17, R20, R22, R24, R26 and R29) on the RTK772100BC00000BR should be removed because the signals from LCD1_DATA0 to LCD1_DATA7 may be affected when the analog RGB output interface (ch1) is used.

Table2.12.1 lists the RTK772100BC00000BR JP6 Function Setting. Figure 2.12.1 and Figure 2.12.2 show the Analog RGB Output Interface Block Diagram. Table2.12.2 lists the SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting, Table2.12.3 lists the RTK772100BC00000BR JP4 Function Setting, and Table2.12.4 lists the JP6, JP7, JP2 and JP3 Function Settings.

Table2.12.1 RTK772100BC00000BR JP6 Function Setting

Jumper	1-2	2-3
JP6	Use P3_7 as LCD1_EXTCLK input pin	Use P3_7 as CS1 output pin (initial setting)

indicates setting function.

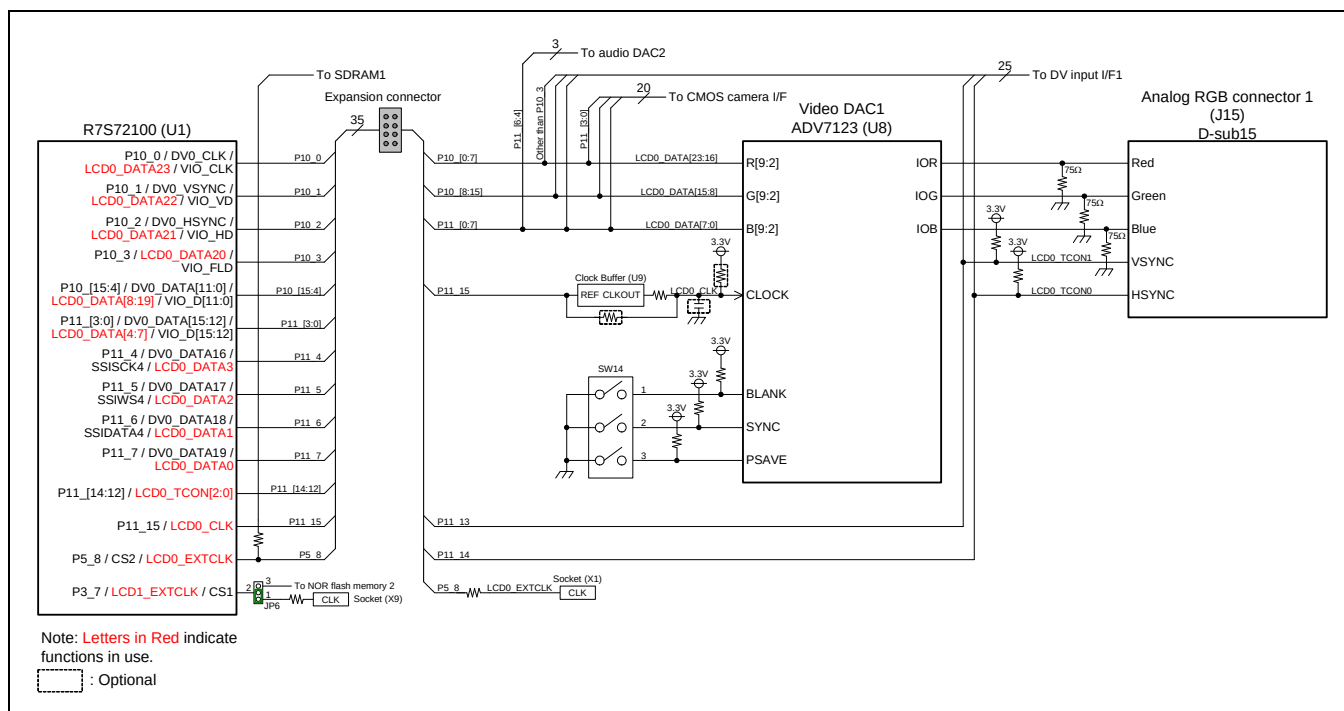


Figure 2.12.1 Analog RGB Output Interface (ch0) Block Diagram

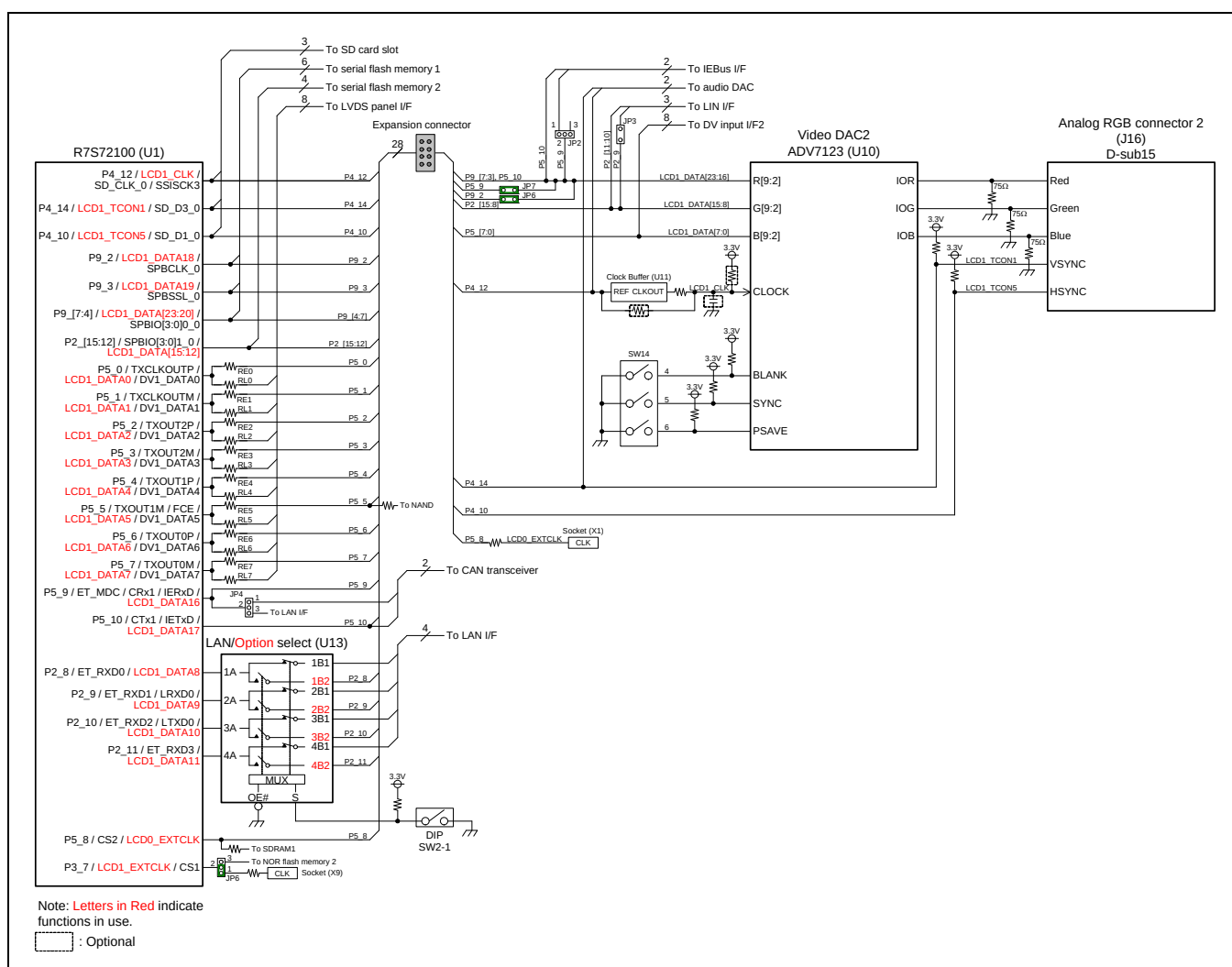


Figure 2.12.2 Analog RGB Output Interface (ch1) Block Diagram

Table 2.12.2 SW2-1 (DIP Switch for RTK772100BC00000BR System Setting) Function Setting

DIP Switch	Function	
	ON	OFF
SW2-1	Use P3_[6:3] and P2_[11:0] as Ethernet PHY control pin (initial setting)	Use P3_[6:3] and P2_[11:0] as MOST control pin and expansion connector pin

indicates setting function.

Table2.12.3 RTK772100BC00000BR JP4 Function Setting

Jumper	1-2	2-3	None
JP4	Use P5_9 as CRx1 input pin	Use P5_9 as ET_MDC output pin (initial setting)	Use P5_9 as IERxD input pin or LCD1_DATA16 output pin

■ indicates setting function.

Table2.12.4 JP6, JP7, JP2 and JP3 Function Settings

Jumper	1-2	2-3 or Open
JP6	Use P9_2 as LCD1_DATA18 output pin	Use P9_2 as SPBCLK_0 output pin (initial setting)
JP7	Use P5_9 as IERxD input pin or LCD1_DATA16 output pin	Use P5_9 as ET_MDC output pin (initial setting)
JP2	Use P5_9 as IERxD input pin	Use P5_9 as LCD1_DATA16 output pin (initial setting)
JP3	Use P2_9 as LRXD0 input pin	Use P2_9 as LCD1_DATA9 output pin (initial setting)

■ indicates setting function.

2.13 Digital Video Signal Input Interface

The R7S72100 has digital video signal input pins (DV pins) respond to the YCbCr422, YCbCr444, RGB888, RGB666 and RGB565 images. The RTK7721000B00000BR connects the R7S72100 DV pins to the general MIL connectors.

The LVDS termination resistors (R315 to R318) or RL0 to RL7 (R14, R16, R17, R20, R22, R24, R26 and R29) should be removed because the signals from DV1_DATA0 to DV1_DATA7 may be affected when the digital video signal input interface (ch1) is used.

Figure 2.13.1 shows the Digital Video Signal Input Interface Block Diagram.

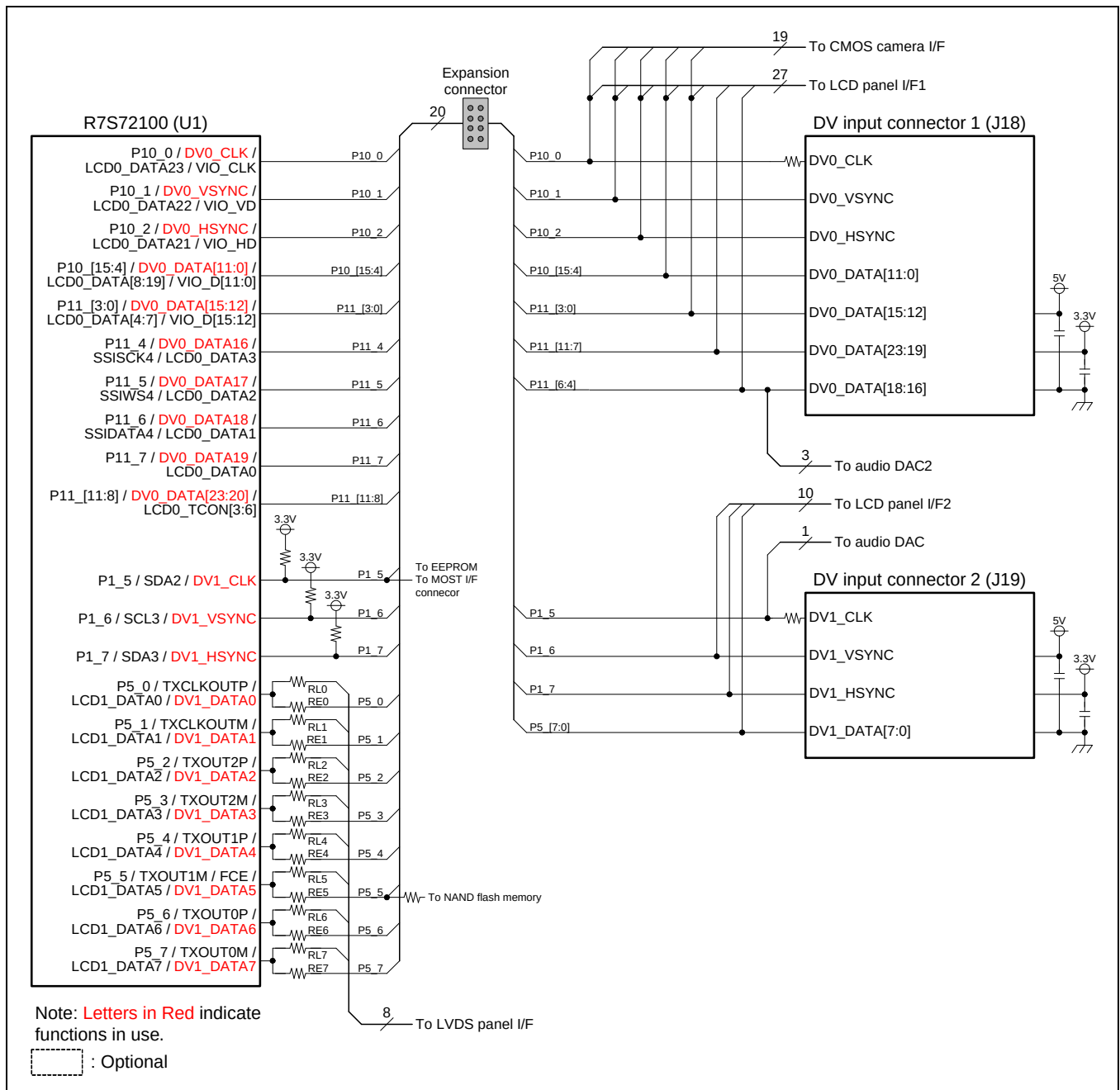


Figure 2.13.1 Digital Video Signal Input Interface Block Diagram

2.14 CMOS Camera Input Interface

The R7S72100 includes a capture module capture engine unit (CEU) which imports video data input from outside and transfers the data to the memory. The RTK7721000B00000BR connects the R7S72100 CEU pin to the CMOS camera connector (MT9V024IA7XTCD ES, Aptina) and the connectable 26-pin MIL pitch connector.

Figure 2.14.1 shows the CMOS Camera Input Interface Block Diagram, Table2.14.1 lists the JP4 Function Setting.

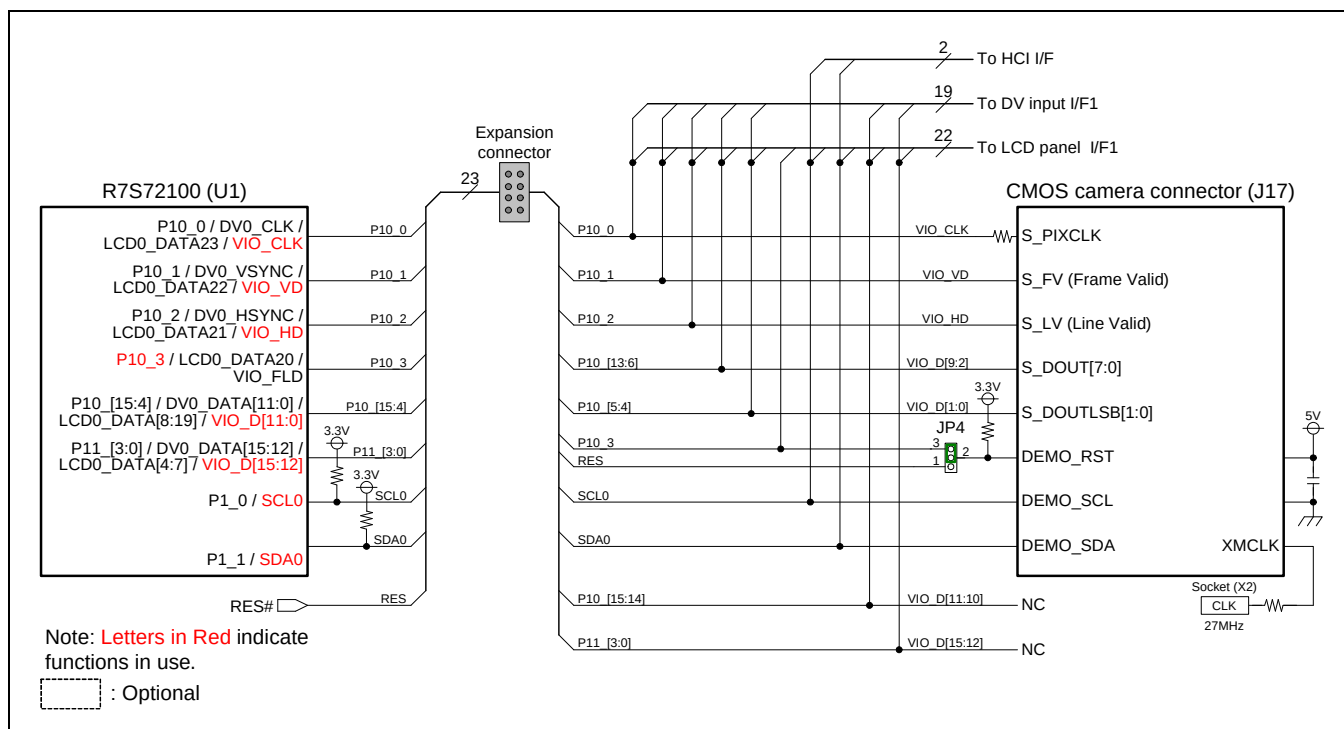


Figure 2.14.1 CMOS Camera Input Interface Block Diagram

Table2.14.1 JP4 Function Setting

Jumper	1-2	2-3
JP4	Execute reset control for CMOS camera using RES signal generated by the RTK7721000B00000BR	Execute reset control for CMOS camera with P10_3 pin (initial setting)

indicates setting function.

2.15 Key Input Switch

The ports from P1_8 to P1_11 can be used as the key input switches via the A/D converter (ADC) by setting to the analog input pins (AN0 to AN3).

Figure 2.15.1 shows the Key Input Switch Block Diagram, and Table2.15.1 lists the Voltage of AD Input Pin and AD value When Pushing Ken Input Switch.

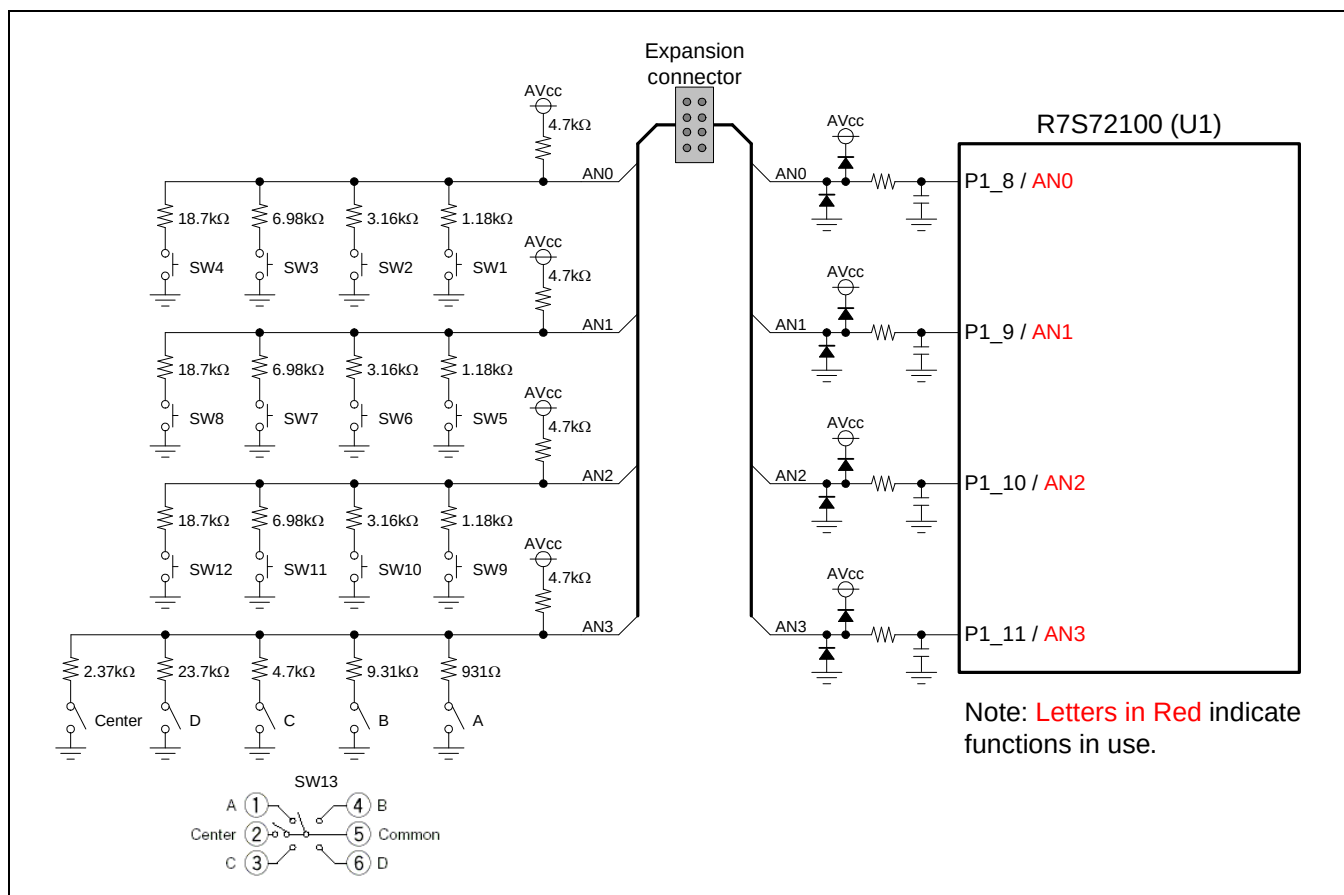


Figure 2.15.1 Key Input Switch Block Diagram

Table2.15.1 Voltage of AD Input Pin and AD value When Pushing Ken Input Switch

Switch	Pin voltage (V)	10-bit AD value	12-bit AD value
SW1, SW5, SW9	0.66	205	822
SW2, SW6, SW10	1.33	412	1647
SW3, SW7, SW11	1.97	612	2448
SW4, SW8, SW12	2.64	818	3273
SW13-A	0.55	169	677
SW13-B	2.19	680	2722
SW13-C	1.65	512	2048
SW13-D	2.75	855	3418
SW13-Center	1.11	343	1373

* Calculated when Avcc is 3.3V, and Avss is 0V. The difference of the resisgors and the voltage is not included.

2.16 Power Configuration

The RTK7721000B00000BR is operated with 12V, 5V, and 3.3V supplied from the RTK772100BC00000BR. Analog 3.3V for the video DAC and the audio DAC and 8V for the CD deck are generated on the RTK7721000B00000BR.

Figure 2.16.1 shows the Power Configuration Diagram.

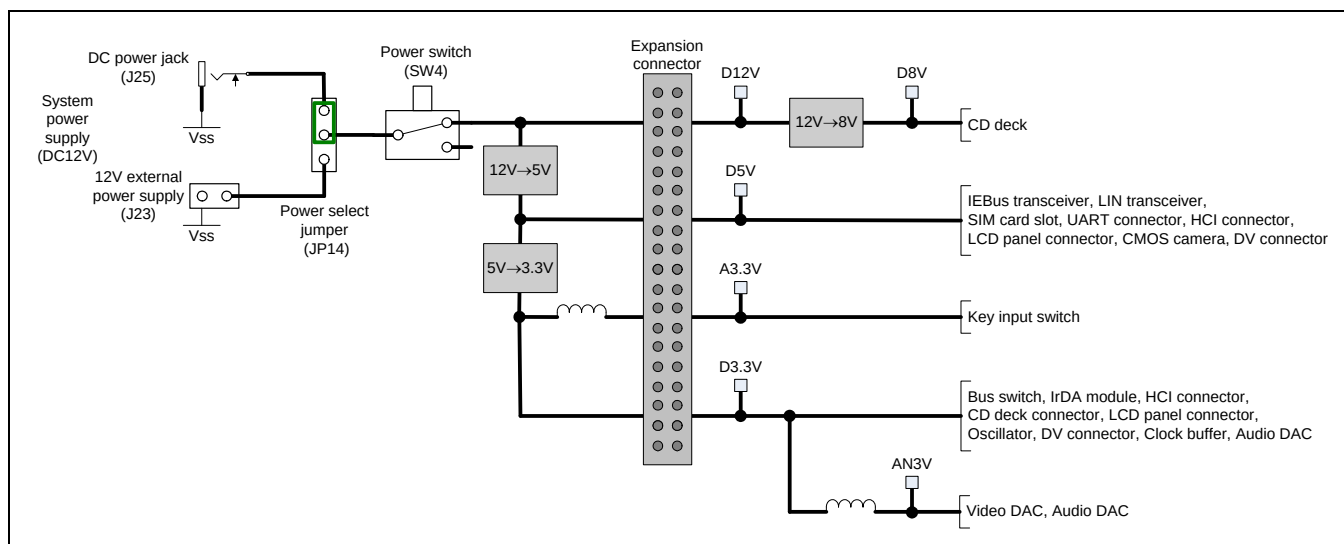


Figure 2.16.1 Power Configuration Diagram

3. Operational Specification

3.1 Connector Overview

Figure 3.1.1 and Figure 3.1.2 show the RTK7721000B00000BR Connector Layouts

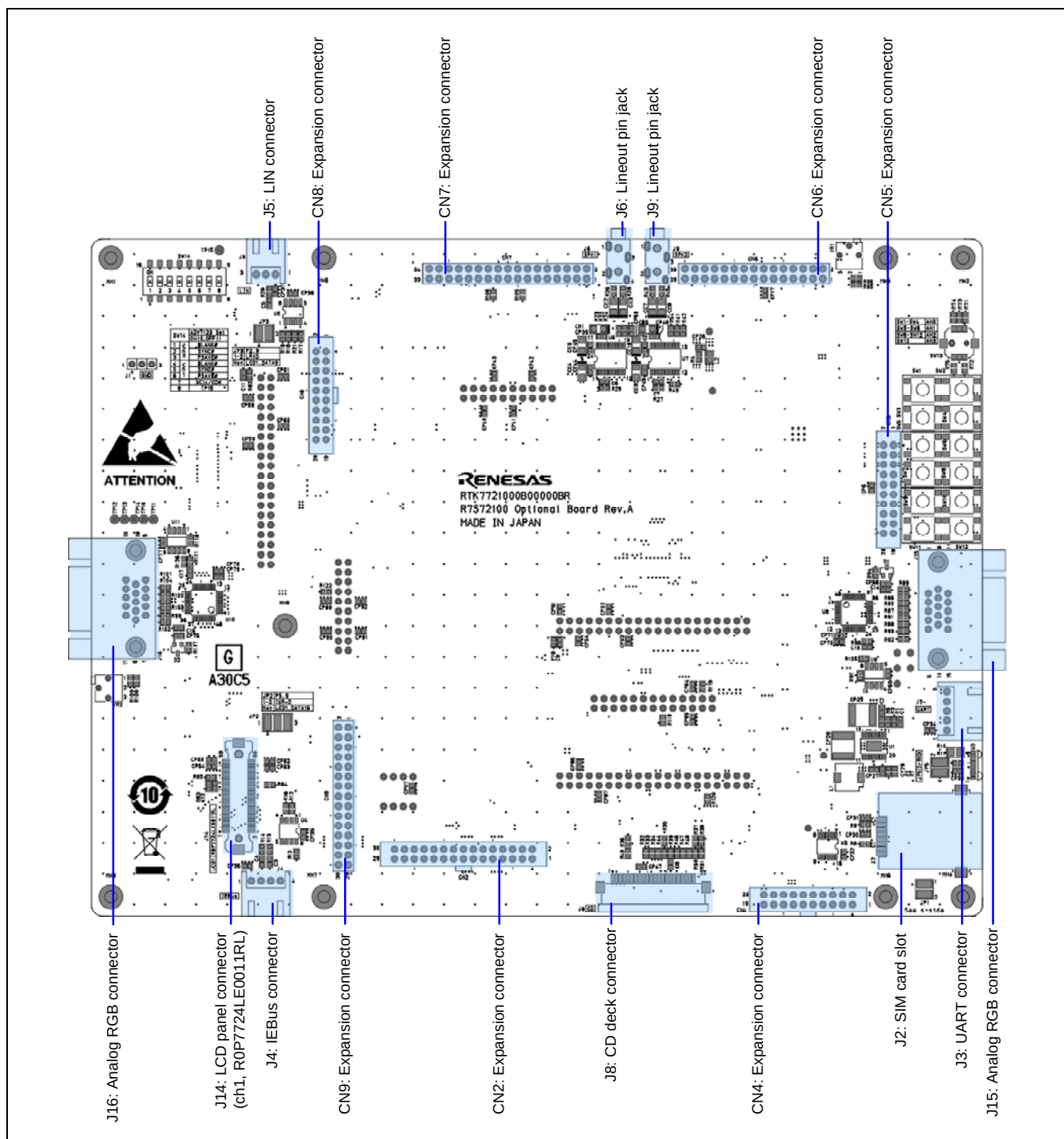


Figure 3.1.1 RTK7721000B00000BR Connector Layout (Top View of Component Side)

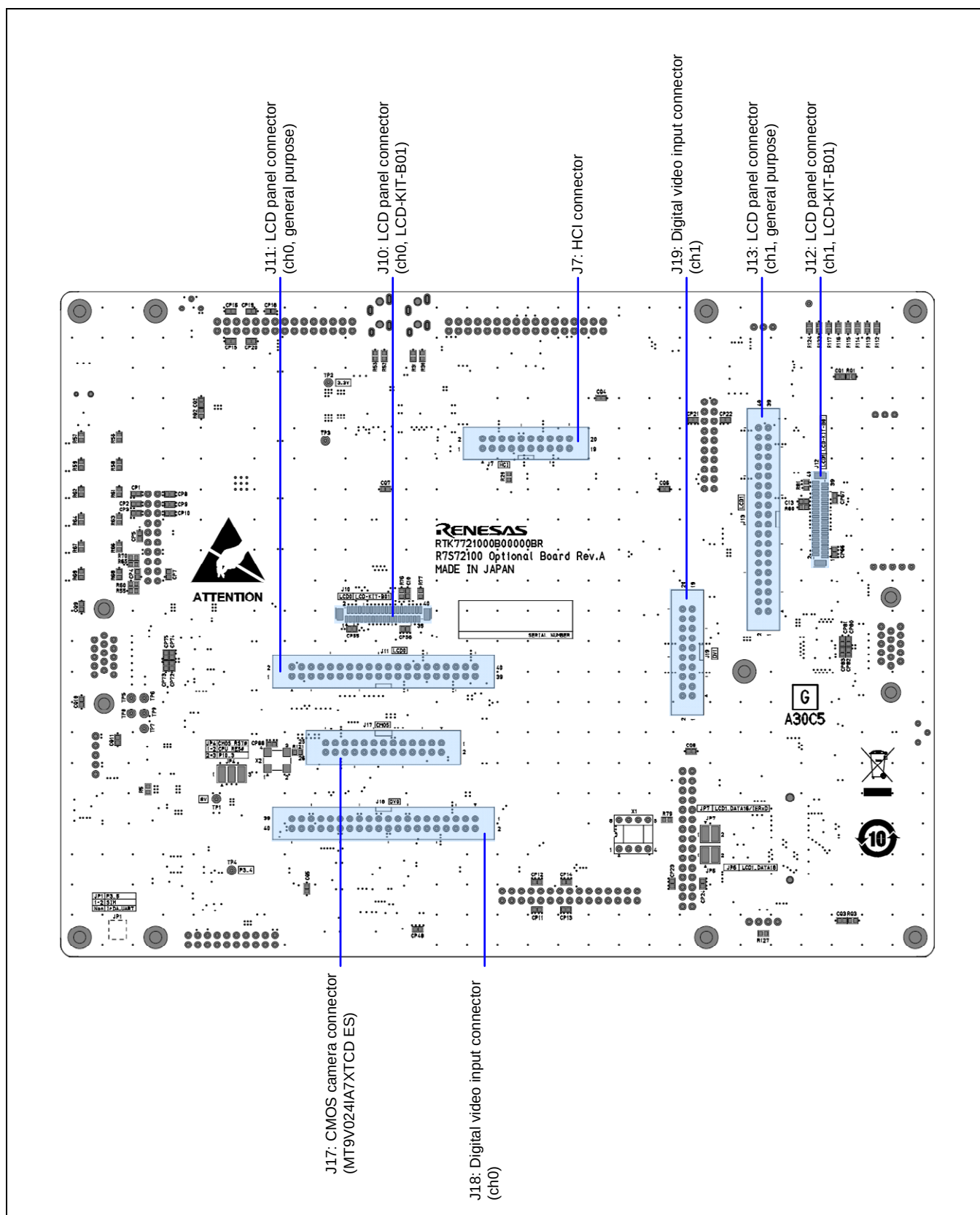


Figure 3.1.2 RTK7721000B00000BR Connector Layout (Top View of Solder Side)

3.1.1 Expansion Connectors (CN1 to CN9)

The RTK7721000B00000BR has expansion connectors (CN2, CN4 to CN9) to connect with the RTK772100BC00000BR. Figure 3.1.3 shows the Pinout Diagram of Expansion Connector, and Table 3.1.1 to Table 3.1.7 list the Expansion Connector Pin Assignments.

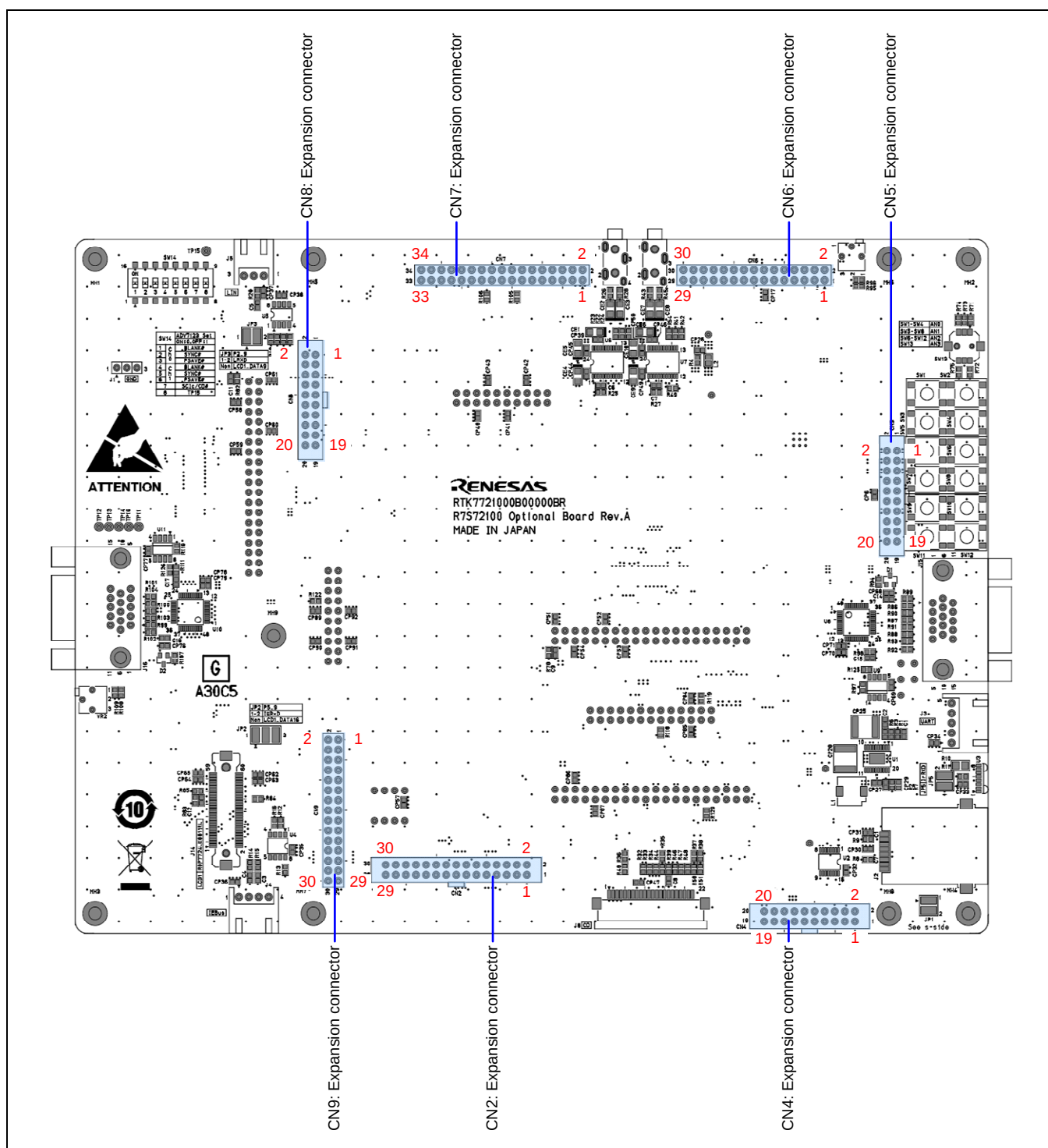


Figure 3.1.3 Pinout Diagram of Expansion Connector

Table 3.1.1 Expansion Connector Pin Assignments 1 (CN2)

Pin No.	Signal Name	Pin No.	Signal Name
1	Vss	2	CKIO
3	Vss	4	Vss
5	P11_11 / DV0_DATA23 / SD_D2_0 / RxD5 / MMC_D2 / LCD0_TCON3	6	P11_10 / DV0_DATA22 / SD_D3_0 / TxD5 / MMC_D3 / LCD0_TCON4
7	P11_9 / DV0_DATA21 / SD_CMD_0 / SCK5 / MMC_CMD / LCD0_TCON5	8	P11_8 / DV0_DATA20 / SD_CLK_0 / RTS5 / MMC_CLK / LCD0_TCON6
9	3VCC	10	3VCC
11	P11_7 / DV0_DATA19 / SD_D0_0 / CTS5 / MMC_D0 / LCD0_DATA0	12	P11_6 / DV0_DATA18 / SD_D1_0 / SSIDATA4 / MMC_D1 / LCD0_DATA1
13	P11_5 / DV0_DATA17 / SD_WP_0 / SSIWS4 / LCD0_DATA2	14	P11_4 / DV0_DATA16 / SD_CD_0 / SSISCK4 / MMC_CD / LCD0_DATA3
15	3VCC	16	3VCC
17	P11_15 / SPDIF_OUT / MISO1 / IRQ1 / MMC_D7 / LCD0_CLK	18	P11_14 / SPDIF_IN / MOSI1 / LCD0_TCON5 / MMC_D6 / LCD0_TCON0
19	P11_13 / CTx1 / SSL10 / LCD0_TCON4 / MMC_D5 / LCD0_TCON1	20	P11_12 / CRx1 / RSPCK1 / IRQ3 / MMC_D4 / LCD0_TCON2
21	Vss	22	P7_8 / RD / SSISCK3 / CRx0 / TIOC3A / IRQ1
23	P7_7 / WE1/DQMLU / DV0_DATA23 / ET_TXD3 / RTS7 / SSIDATA2 / TIOC2B	24	P7_6 / WE0/DQMLL / DV0_DATA22 / ET_TXD2 / CTS7 / SSIWS2 / TIOC2A
25	P7_5 / RD/WR / DV0_DATA21 / ET_TXD1 / RXD7 / SSISCK2 / TIOC1B	26	P7_4 / CKE / DV0_DATA20 / ET_TXD0 / TXD7 / SSITxD1 / TIOC1A
27	P7_3 / CAS / DV0_DATA19 / ET_TXEN / SCK7 / CTx2 / SSIRxD1 / TIOC0D	28	P7_2 / RAS / DV0_DATA18 / ET_TXER / RXD4 / CRx2 / SSIWS1 / TIOC0C
29	P7_1 / CS3 / DV0_DATA17 / ET_TXCLK / TXD4 / DV0_CLK / SSISCK1 / TIOC0B	30	P7_0 / MD_BOOT2 / CS0 / DV0_DATA16 / ET_MDC / SCK4 / LTXD0 / TIOC0A

: 5V system power supply,
 : 3.3V system power supply,
 : GND

Table 3.1.2 Expansion Connector Pin Assignments 2 (CN4)

Pin No.	Signal Name	Pin No.	Signal Name
1	NMI	2	RES#
3	NC	4	NC
5	P3_1 / LCD0_TCON0 / ET_TXER / IRQ6 / TxD2 / SCI_TXD1 / AUDIO_CLK / PWM2B / SSL30	6	P3_0 / LCD0_CLK / ET_TXCLK / IRQ2 / SCK2 / SCI_SCK1 / TxD2 / PWM2A / RSPCK3
7	P3_3 / LCD0_TCON2 / ET_MDIO / IRQ4 / BS / SCI_CTS1 / RTS1 / DACK0 / PWM2D / MISO3	8	P3_2 / LCD0_TCON1 / ET_TXEN / RxD2 / SCI_RXD1 / TEND0 / PWM2C / MOSI3
9	Vss	10	Vss
11	P3_5 / LCD0_TCON4 / ET_RXER / SSIWS1 / AUDIO_XOUT3 / SCI_TXD0 / TIOC3B / TxD3	12	P3_4 / LCD0_TCON3 / ET_RXCLK / SSISCK1 / AUDIO_XOUT2 / SCI_SCK0 / TIOC3A / SCK3
13	P3_7 / LCD0_TCON6 / SSITxD1 / LCD1_EXTCLK / SCI_CTS0/RTS0 / TIOC3D / CS1 / WDTOVF	14	P3_6 / LCD0_TCON5 / ET_RXDV / SSIRxD1 / SCI_RXD0 / TIOC3C / RxD3
15	Vss	16	Vss
17	P10_3 / TCLKD / PWM2D / ET_CRS / LCD0_DATA20 / VIO_FLD	18	P10_2 / DV0_HSYNC / TCLKC / PWM2C / ET_TXEN / LCD0_DATA21 / VIO_HD
19	P10_1 / DV0_VSYNC / TCLKB / PWM2B / ET_TXER / LCD0_DATA22 / VIO_VD	20	P10_0 / DV0_CLK / TCLKA / PWM2A / ET_TXCLK / LCD0_DATA23 / VIO_CLK

: 5V system power supply,
 : 3.3V system power supply,
 : GND

Table 3.1.3 Expansion Connector Pin Assignments 3 (CN5)

Pin No.	Signal Name	Pin No.	Signal Name
1	+12V	2	+12V
3	+12V	4	+12V
5	+12V	6	+12V
7	P1_15 / AN7	8	P1_14 / AN6 / ET_COL
9	AVcc	10	AVcc
11	P1_13 / AN5 / DV0_HSYNC / WAIT	12	P1_12 / AN4 / DV0_VSYNC / VIO_FLD
13	AVss	14	AVss
15	P1_11 / AN3 / IRQ5 / TCLKD	16	P1_10 / AN2 / IRQ4 / TCLKB
17	VBUS	18	VBUS
19	P1_9 / AN1 / IRQ3 / VIO_D15 / DV0_DATA15	20	P1_8 / AN0 / IRQ2 / DREQ0 / VIO_D14 / DV0_DATA14

: 5V system power supply,
 : 3.3V system power supply,
 : GND

Table 3.1.4 Expansion Connector Pin Assignments 4 (CN6)

Pin No.	Signal Name	Pin No.	Signal Name
1	P3_9 / LCD0_DATA1 / NAF1 / TRACEDATA1 / TIOC4B / SD_WP_1 / IRQ6	2	P3_8 / LCD0_DATA0 / NAF0 / TRACEDATA0 / TIOC4A / SD_CD_1 / MMC_CD
3	P3_11 / LCD0_DATA3 / NAF3 / TRACEDATA3 / TIOC4D / SD_D0_1 / MMC_D0	4	P3_10 / LCD0_DATA2 / NAF2 / TRACEDATA2 / TIOC4C / SD_D1_1 / MMC_D1
5	5VCC	6	5VCC
7	5VCC	8	5VCC
9	P3_13 / LCD0_DATA5 / NAF5 / AUDIO_XOUT / SD_CMD_1 / MMC_CMD	10	P3_12 / LCD0_DATA4 / NAF4 / SD_CLK_1 / MMC_CLK
11	P3_15 / LCD0_DATA7 / NAF7 / TRACECTRL / SD_D2_1 / MMC_D2	12	P3_14 / LCD0_DATA6 / NAF6 / TRACECLK / SD_D3_1 / MMC_D3
13	3VCC	14	3VCC
15	P4_1 / LCD0_DATA9 / TIOC0B / FCLE / SCK2 / SSL40 / MMC_D5	16	P4_0 / LCD0_DATA8 / TIOC0A / FRE / RSPCK4 / MMC_D4
17	P4_3 / LCD0_DATA11 / TIOC0D / FWE / CTx3 / RxD2 / MISO4 / MMC_D7	18	P4_2 / LCD0_DATA10 / TIOC0C / FALE / CRx3 / TxD2 / MOSI4 / MMC_D6
19	Vss	20	Vss
21	P10_5 / DV0_DATA1 / TIOC0B / PWM2F / ET_TXD1 / LCD0_DATA18 / VIO_D1	22	P10_4 / DV0_DATA0 / TIOC0A / PWM2E / ET_TXD0 / LCD0_DATA19 / VIO_D0
23	P10_7 / DV0_DATA3 / TIOC0D / PWM2H / ET_TXD3 / LCD0_DATA16 / VIO_D3	24	P10_6 / DV0_DATA2 / TIOC0C / PWM2G / ET_TXD2 / LCD0_DATA17 / VIO_D2
25	Vss	26	Vss
27	P4_5 / LCD0_DATA13 / SSL10 / TIOC4B / PWM2F / SSIWS0 / DV0_DATA13	28	P4_4 / LCD0_DATA12 / RSPCK1 / TIOC4A / PWM2E / SSISCK0 / DV0_DATA12
29	P4_7 / LCD0_DATA15 / MISO1 / TIOC4D / PWM2H / SSITxD0 / DV0_DATA15	30	P4_6 / LCD0_DATA14 / MOSI1 / TIOC4C / PWM2G / SSIRxD0 / DV0_DATA14

: 5V system power supply,
 : 3.3V system power supply,
 : GND

Table 3.1.5 Expansion Connector Pin Assignments 5 (CN7)

Pin No.	Signal Name	Pin No.	Signal Name
1	AUDIO_XTAL1	2	AUDIO_XTAL2
3	Vss	4	Vss
5	P10_9 / DV0_DATA5 / TIOC1B / ET_RXD1 / LCD0_DATA14 / VIO_D5	6	P10_8 / DV0_DATA4 / TIOC1A / ET_RXD0 / LCD0_DATA15 / VIO_D4
7	P10_11 / DV0_DATA7 / TIOC2B / ET_RXD3 / LCD0_DATA12 / VIO_D7	8	P10_10 / DV0_DATA6 / TIOC2A / ET_RXD2 / LCD0_DATA13 / VIO_D6
9	P10_13 / DV0_DATA9 / SSIWS1 / SSL00 / LCD0_DATA10 / VIO_D9	10	P10_12 / DV0_DATA8 / SSISCK1 / RSPCK0 / LCD0_DATA11 / VIO_D8
11	P10_15 / DV0_DATA11 / SSITxD1 / MISO0 / LCD0_DATA8 / VIO_D11	12	P10_14 / DV0_DATA10 / SSIRxD1 / MOSI0 / LCD0_DATA9 / VIO_D10
13	P4_9 / LCD0_DATA17 / LCD1_TCON4 / SD_WP_0 / SSIWS5 / CRx2 / TxD0 / IRQ1	14	P4_8 / LCD0_DATA16 / LCD1_TCON3 / SD_CD_0 / MMC_CD / SSISCK5 / CTx2 / SCK0 / IRQ0
15	P4_11 / LCD0_DATA19 / LCD1_TCON6 / SD_D0_0 / MMC_D0 / SSITxD5 / CTx4 / SCK1 / IRQ3	16	P4_10 / LCD0_DATA18 / LCD1_TCON5 / SD_D1_0 / MMC_D1 / SSIRxD5 / RxD0 / IRQ2
17	P4_13 / LCD0_DATA21 / LCD1_TCON0 / SD_CMD_0 / MMC_CMD / SPBIO11_1 / SSIWS3 / RxD1 / IRQ5	18	P4_12 / LCD0_DATA20 / LCD1_CLK / SD_CLK_0 / MMC_CLK / SPBIO10_1 / SSISCK3 / TxD1 / IRQ4
19	P4_15 / LCD0_DATA23 / LCD1_TCON2 / SD_D2_0 / MMC_D2 / SPBIO31_1 / SSITxD3 / RxD2 / IRQ7	20	P4_14 / LCD0_DATA22 / LCD1_TCON1 / SD_D3_0 / MMC_D3 / SPBIO21_1 / SSIRxD3 / TxD2 / IRQ6
21	Vss	22	Vss
23	P2_1 / D17 / ET_TXER / DV0_DATA1 / SPBIO10_1 / MLB_DAT / TIOC2A / VIO_D1 / LCD0_DATA17	24	P2_0 / D16 / ET_TXCLK / DV0_DATA0 / SPBIO00_1 / MLB_CLK / IRQ5 / VIO_D0 / LCD0_DATA16
25	P2_3 / D19 / ET_CRS / DV0_DATA3 / SPBIO30_1 / IERxD / CTS1 / VIO_D3 / LCD0_DATA19	26	P2_2 / D18 / ET_TXEN / DV0_DATA2 / SPBIO20_1 / MLB_SIG / TIOC2B / VIO_D2 / LCD0_DATA18
27	P2_5 / D21 / ET_TXD1 / DV0_DATA5 / SSIWS5 / SPBSSL_1 / TxD1 / VIO_D5 / LCD0_DATA21	28	P2_4 / D20 / ET_TXD0 / DV0_DATA4 / SSISCK5 / SPBCLK_1 / SCK1 / VIO_D4 / LCD0_DATA20
29	P2_7 / D23 / ET_TXD3 / DV0_DATA7 / SSITxD5 / IETxD / RTS1 / VIO_D7 / LCD0_DATA23	30	P2_6 / D22 / ET_TXD2 / DV0_DATA6 / SSIRxD5 / RxD1 / VIO_D6 / LCD0_DATA22
31	P2_9 / D25 / ET_RXD1 / DV0_DATA9 / SSIWS0 / LRXD0 / LCD1_DATA9 / VIO_D9 / SSL40	32	P2_8 / D24 / ET_RXD0 / DV0_DATA8 / SSISCK0 / LCD0_TCON6 / LCD1_DATA8 / VIO_D8 / RSPCK4
33	P2_11 / D27 / ET_RXD3 / DV0_DATA11 / SSITxD0 / TIOC1A / LCD1_DATA11 / VIO_D11 / MISO4	34	P2_10 / D26 / ET_RXD2 / DV0_DATA10 / SSIRxD0 / LTxD0 / LCD1_DATA10 / VIO_D10 / MOSI4

: 5V system power supply,
 : 3.3V system power supply,
 : GND

Table 3.1.6 Expansion Connector Pin Assignments 6 (CN8)

Pin No.	Signal Name	Pin No.	Signal Name
1	P3_4 / LCD0_TCON3 / ET_RXCLK / SSISCK1 / AUDIO_XOUT2 / SCI_SCK0 / TIOC3A / SCK3	2	P3_3 / LCD0_TCON2 / ET_MDIO / IRQ4 / BS / SCI_CTS1 / RTS1 / DACK0 / PWM2D / MISO3
3	P3_6 / LCD0_TCON5 / ET_RXDV / SSIRxD1 / SCI_RXD0 / TIOC3C / RxD3	4	P3_5 / LCD0_TCON4 / ET_RXER / SSIWS1 / AUDIO_XOUT3 / SCI_TXD0 / TIOC3B / TxD3
5	3VCC	6	3VCC
7	P2_13 / D29 / SSL00 / DV0_DATA13 / SPBIO11_0 / CTx3 / SCK0 / LCD1_DATA13 / IRQ7	8	P2_12 / D28 / RSPCK0 / DV0_DATA12 / SPBIO01_0 / CRx3 / IRQ6 / LCD1_DATA12 / TIOC1B
9	P2_15 / D31 / MISO0 / DV0_DATA15 / SPBIO31_0 / CAN_CLK / RxD0 / LCD1_DATA15 / IRQ1	10	P2_14 / D30 / MOSI0 / DV0_DATA14 / SPBIO21_0 / CRx4 / TxD0 / LCD1_DATA14 / IRQ0
11	Vss	12	Vss
13	P1_1 / SDA0 / DV0_DATA17 / TCLKC / IRQ1 / VIO_HD / DV0_HSYNC	14	P1_0 / SCL0 / DV0_DATA16 / TCLKA / IRQ0 / VIO_VD / DV0_VSYNC
15	P1_3 / SDA1 / DV0_DATA19 / ET_COL / IRQ3 / ADTRG	16	P1_2 / SCL1 / DV0_DATA18 / FRB / IRQ2 / LCD1_EXTCLK
17	P1_5 / SDA2 / DV1_CLK / CRx4 / IRQ5 / VIO_CLK / LCD1_EXTCLK	18	P1_4 / SCL2 / DV0_CLK / CRx1 / IRQ4 / CAN_CLK
19	P1_7 / SDA3 / DV1_HSYNC / LRxD0 / IRQ7 / VIO_D13 / DV0_DATA13	20	P1_6 / SCL3 / DV1_VSYNC / IERxD / IRQ6 / VIO_D12 / DV0_DATA12

: 5V system power supply,
 : 3.3V system power supply,
 : GND

Table 3.1.7 Expansion Connector Pin Assignments 7 (CN9)

Pin No.	Signal Name	Pin No.	Signal Name
1	P5_1 / TXCLKOUTM / LCD1_DATA1 / LCD0_DATA17 / DV1_DATA1 / RxD4 / TIOC0B / SSL30	2	P5_0 / TXCLKOUTP / LCD1_DATA0 / LCD0_DATA16 / DV1_DATA0 / TxD4 / TIOC0A / RSPCK3
3	P5_3 / TXOUT2M / LCD1_DATA3 / LCD0_DATA19 / DV1_DATA3 / TxD3 / TIOC3C / MISO3	4	P5_2 / TXOUT2P / LCD1_DATA2 / LCD0_DATA18 / DV1_DATA2 / SCK3 / TIOC1B / MOSI3
5	P5_5 / TXOUT1M / LCD1_DATA5 / LCD0_DATA21 / DV1_DATA5 / AUDIO_XOUT / TIOC0C / FCE / DV0_DATA13	6	P5_4 / TXOUT1P / LCD1_DATA4 / LCD0_DATA20 / DV1_DATA4 / RxD3 / TIOC3D / DV0_DATA12
7	P5_7 / TXOUT0M / LCD1_DATA7 / LCD0_DATA23 / DV1_DATA7 / RxD6 / TIOC0D / SPDIF_OUT / DV0_DATA15	8	P5_6 / TXOUT0P / LCD1_DATA6 / LCD0_DATA22 / DV1_DATA6 / TxD6 / IRQ6 / SPDIF_IN / DV0_DATA14
9	Vss	10	Vss
11	P5_8 / LCD0_EXTCLK / IRQ0 / DV1_CLK / DV0_CLK / CS2	12	Vss
13	Vss	14	Vss
15	P5_10 / WE3/DQM0U/AH / DV0_HSYNC / CTx1 / IETxD / LCD1_DATA17	16	P5_9 / WE2/DQMUL / ET_MDC / DV0_VSYNC / IRQ2 / CRx1 / IERxD / LCD1_DATA16
17	Vss	18	Vss
19	P9_3 / LCD1_DATA19 / SPBSSL_0 / TxD1	20	P9_2 / LCD1_DATA18 / SPBCLK_0 / LTXD0 / SCK1 / A0
21	P9_5 / LCD1_DATA21 / SPBIO10_0 / SSISCK2 / CTS1 / CS4	22	P9_4 / LCD1_DATA20 / SPBIO00_0 / RxD1
23	P9_7 / LCD1_DATA23 / SPBIO30_0 / SSIDATA2 / TIOC1A	24	P9_6 / LCD1_DATA22 / SPBIO20_0 / SSIWS2 / RTS1 / CS5
25	3VCC	26	3VCC
27	P11_1 / DV0_DATA13 / TIOC4B / TxD6 / LCD0_DATA6 / VIO_D13	28	P11_0 / DV0_DATA12 / TIOC4A / SCK6 / LCD0_DATA7 / VIO_D12
29	P11_3 / DV0_DATA15 / TIOC4D / LCD0_DATA4 / VIO_D15	30	P11_2 / DV0_DATA14 / TIOC4C / RxD6 / LCD0_DATA5 / VIO_D14

: 5V system power supply,
 : 3.3V system power supply,
 : GND

3.1.2 SIM Card Slot (J2)

The RTK7721000B00000BR has a SIM card slot (J2).

Figure 3.1.4 shows the Pinout Diagram of SIM Card Slot, and Table 3.1.8 lists the SIM Card Slot Pin Assignments.

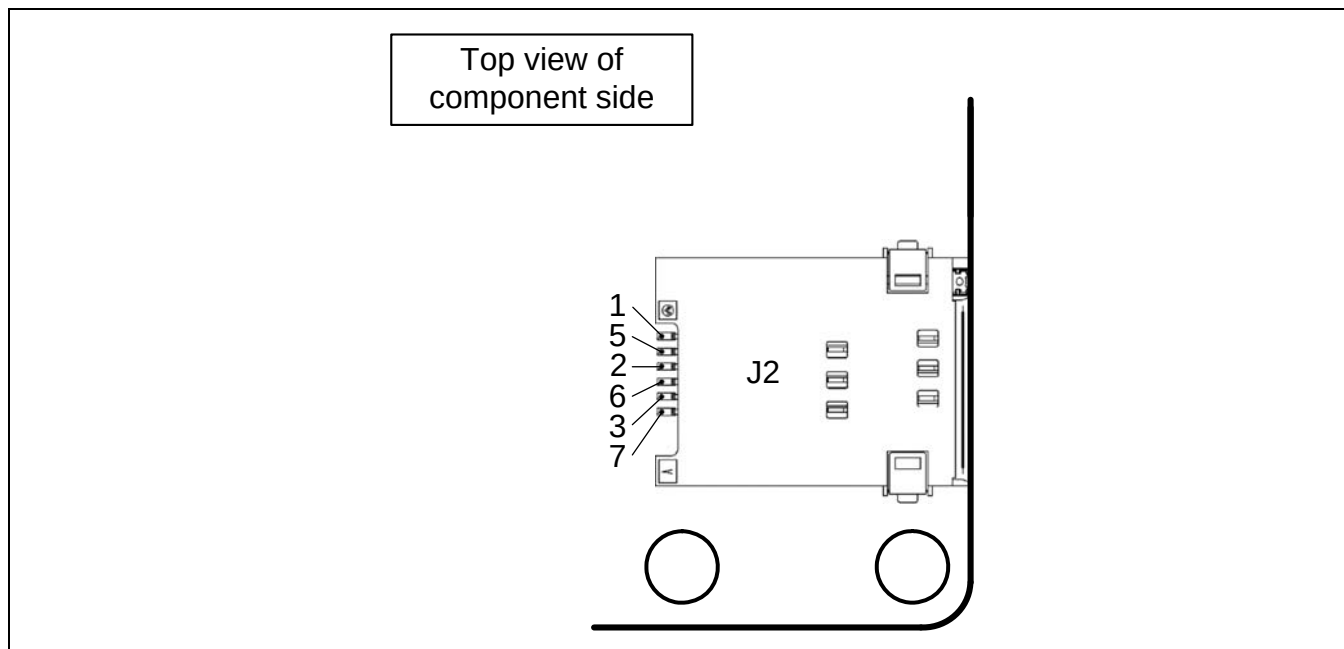


Figure 3.1.4 Pinout Diagram of SIM Card Slot

Table 3.1.8 SIM Card Slot Pin Assignments

Pin No.	Signal Name
1	+5V
2	RST (P3_3 / LCD0_TCON2 / ET_MDIO / IRQ4 / BS / SCI_CTS1 / RTS1 / DACK0 / PWM2D / MISO3)
3	CLK (P3_4 / LCD0_TCON3 / ET_RXCLK / SSISCK1 / AUDIO_XOUT2 / SCI_SCK0 / TIOC3A / SCK3)
4	NC (without pins)
5	GND (Vss)
6	+3.3V
7	I/O (P3_5 / LCD0_TCON4 / ET_RXER / SSIWS1 / AUDIO_XOUT3 / SCI_TXD0 / TIOC3B / TxD3, and P3_6 / LCD0_TCON5 / ET_RXDV / SSIRxD1 / SCI_RXD0 / TIOC3C / RxD3)
8	NC (without pins)

Note: Bold letters indicate setting functions

3.1.3 UART Connector (J3)

The RTK7721000B00000BR has a UART connector (J3).

Figure 3.1.5 shows the Pinout Diagram of UART Connector, and Table 3.1.9 lists the UART Connector Pin Assignments.

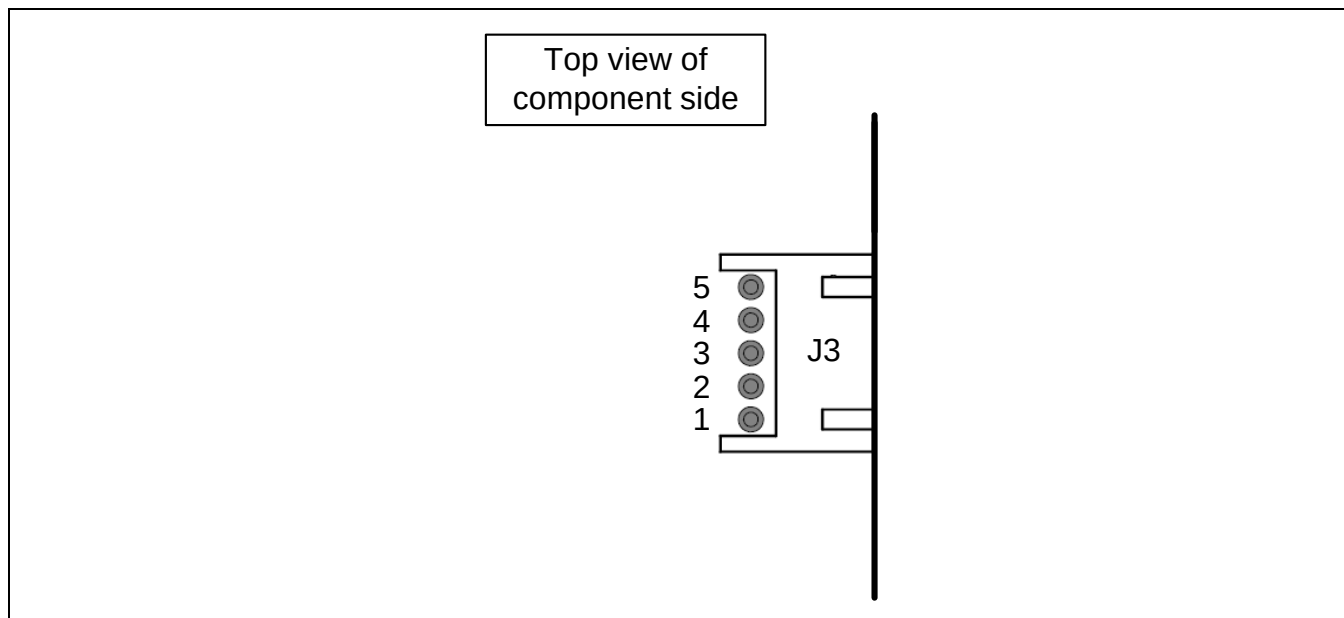


Figure 3.1.5 Pinout Diagram of UART Connector

Table 3.1.9 UART Connector Pin Assignments

Pin No.	Signal Name
1	+5V
2	SCK (P3_4 / LCD0_TCON3 / ET_RXCLK / SSISCK1 / AUDIO_XOUT2 / SCI_SCK0 / TIOC3A / SCK3)
3	TXD (P3_5 / LCD0_TCON4 / ET_RXER / SSIWS1 / AUDIO_XOUT3 / SCI_TXD0 / TIOC3B / TxD3)
4	RXD (P3_6 / LCD0_TCON5 / ET_RXDV / SSIRxD1 / SCI_RXD0 / TIOC3C / RxD3)
5	GND (Vss)

Note: Bold letters indicate setting functions

3.1.4 IEBus Connector (J4)

The RTK7721000B00000BR has an IEBus connector (J4).

Figure 3.1.6 shows the Pinout Diagram of IEBus Connector, and Table 3.1.10 lists the IEBus Connector Pin Assignments.

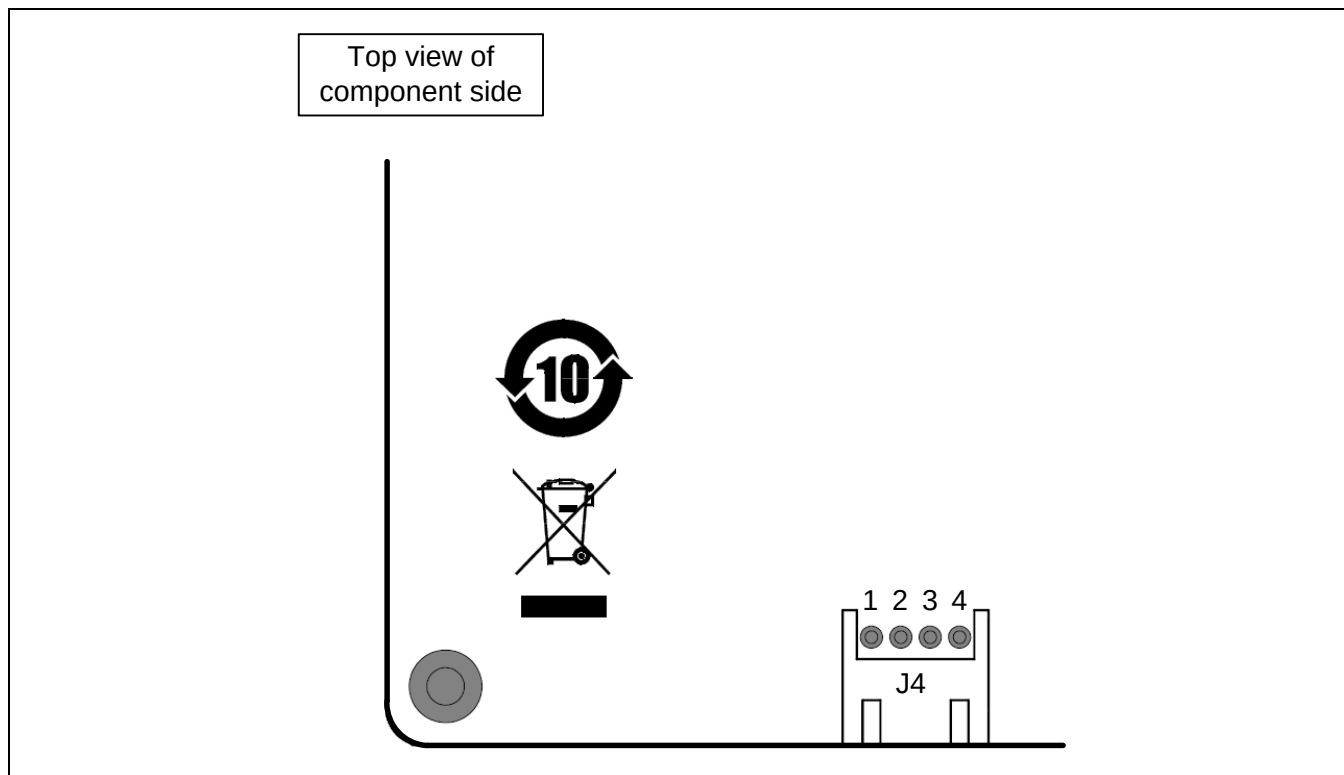


Figure 3.1.6 Pinout Diagram of IEBus Connector

Table 3.1.10 IEBus Connector Pin Assignments

Pin No.	Signal Name
1	+5V
2	BUS+
3	BUS-
4	GND (Vss)

3.1.5 LIN Connector (J5)

The RTK7721000B00000BR has a LIN connector (J5).

Figure 3.1.7 shows the Pinout Diagram of LIN Connector, and Table 3.1.11 lists the LIN Connector Pin Assignments.

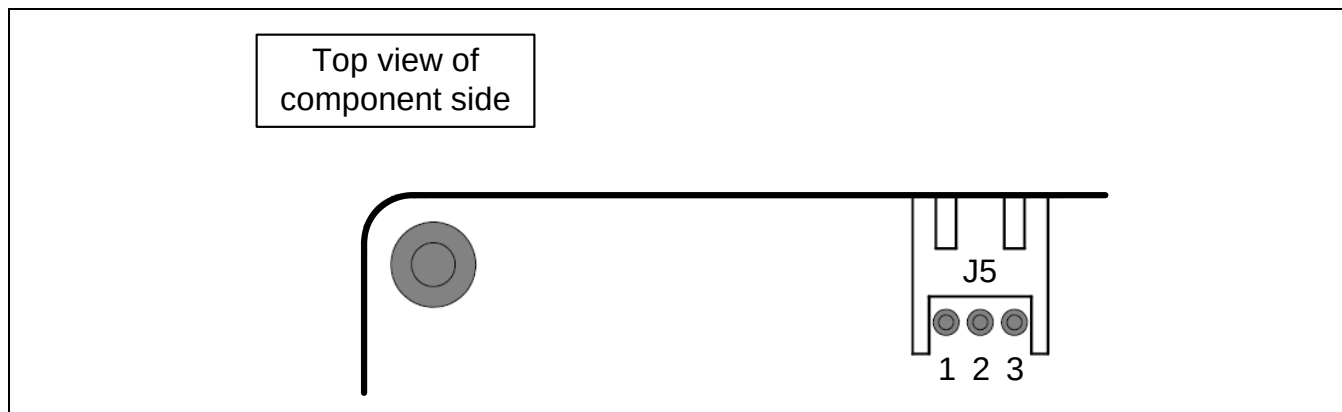


Figure 3.1.7 Pinout Diagram of LIN Connector

Table 3.1.11 LIN Connector Pin Assignments

Pin No.	Signal Name
1	+5V
2	LIN
3	GND (Vss)

3.1.6 Lineout Pin Jacks (J6 and J9)

The RTK7721000B00000BR has two lineout pin jacks (J6 and J9).

Figure 3.1.8 shows the Pinout Diagram of Lineout Pin Jacks, and Table 3.1.12 lists the Lineout Pin Jack Pin Assignments.

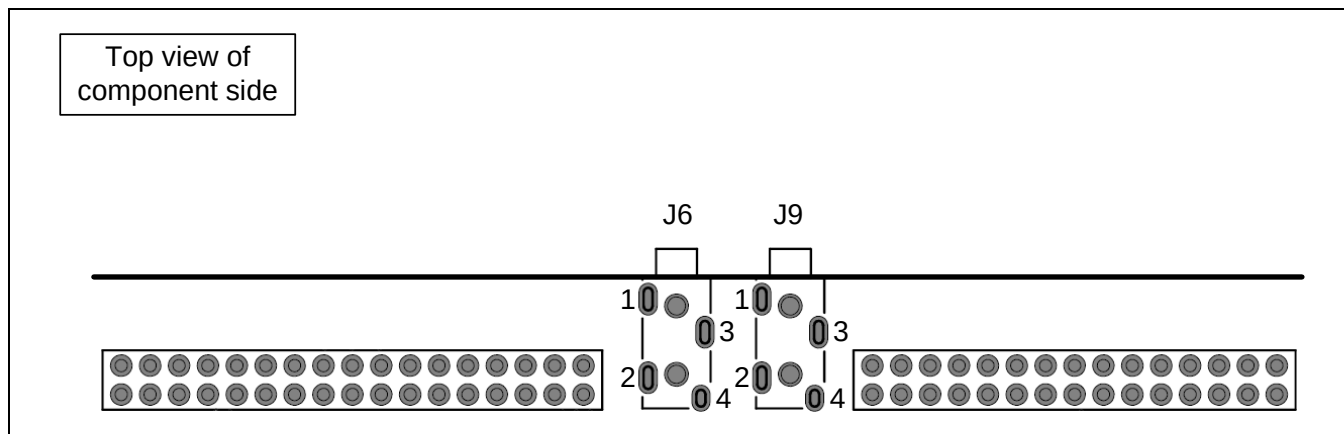


Figure 3.1.8 Pinout Diagram of Lineout Pin Jacks

Table 3.1.12 Lineout Pin Jack Pin Assignments

Pin No.	Signal Name	
	J6	J9
1	GND (AVss)	GND (AVss)
2	AOUTL (Lch analog output pin of audio DAC 1)	AOUTL (Lch analog output pin of audio DAC 2)
3	AOUTR (Rch analog output pin of audio DAC 1)	AOUTR (Rch analog output pin of audio DAC 2)
4	NC	NC

3.1.7 HCI Connector (J7)

The RTK7721000B00000BR has an HCI connector (J7).

Figure 3.1.9 shows the Pinout Diagram of HCI Connector, and Table 3.1.13 lists the HCI Connector Pin Assignments.

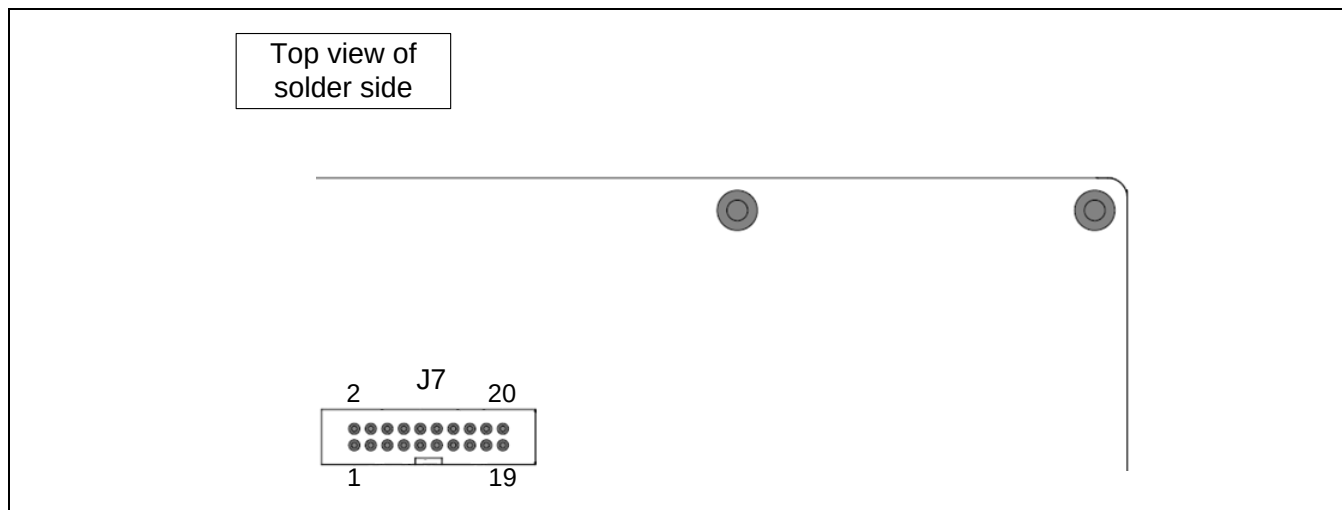


Figure 3.1.9 Pinout Diagram of HCI Connector

Table 3.1.13 HCI Connector Pin Assignments

Pin No.	Signal Name	Pin No.	Signal Name
1	AUDIO_XOUT	2	GND (Vss)
3	GND (Vss)	4	P3_1 / LCD0_TCON0 / ET_TXER / IRQ6 / TxD2 / SCI_TXD1 / AUDIO_CLK / PWM2B / SSL30
5	P1_0 / SCL0 / DV0_DATA16 / TCLKA / IRQ0 / VIO_VD / DV0_VSYNC	6	+3.3V
7	P1_1 / SDA0 / DV0_DATA17 / TCLKC / IRQ1 / VIO_HD / DV0_HSYNC	8	P7_8 / RD / SSISCK3 / CRx0 / TIOC3A / IRQ1
9	+3.3V	10	P2_4 / D20 / ET_TXD0 / DV0_DATA4 / SSISCK5 / SPBCLK_1 / SCK1 / VIO_D4 / LCD0_DATA20
11	P2_5 / D21 / ET_TXD1 / DV0_DATA5 / SSIWS5 / SPBSSL_1 / TxD1 / VIO_D5 / LCD0_DATA21	12	P2_6 / D22 / ET_TXD2 / DV0_DATA6 / SSIRxD5 / RxD1 / VIO_D6 / LCD0_DATA22
13	P2_7 / D23 / ET_TXD3 / DV0_DATA7 / SSITxD5 / IETxD / RTS1 / VIO_D7 / LCD0_DATA23	14	+5V
15	+5V	16	P7_6 / WE0/DQMLL / DV0_DATA22 / ET_TXD2 / CTS7 / SSIWS2 / TIOC2A
17	P7_7 / WE1/DQMLU / DV0_DATA23 / ET_TXD3 / RTS7 / SSIDATA2 / TIOC2B	18	P7_5 / RD/WR / DV0_DATA21 / ET_TXD1 / RxD7 / SSISCK2 / TIOC1B
19	P7_4 / CKE / DV0_DATA20 / ET_TXD0 / TXD7 / SSITxD1 / TIOC1A	20	GND (Vss)

Note: Bold letters indicate setting functions

3.1.8 CD Deck Connector (J8)

The RTK7721000B00000BR has a CD deck connector (J8).

Figure 3.1.10 shows the Pinout Diagram of CD Deck Connector, and Table 3.1.14 lists the CD Deck Connector Pin Assignments.

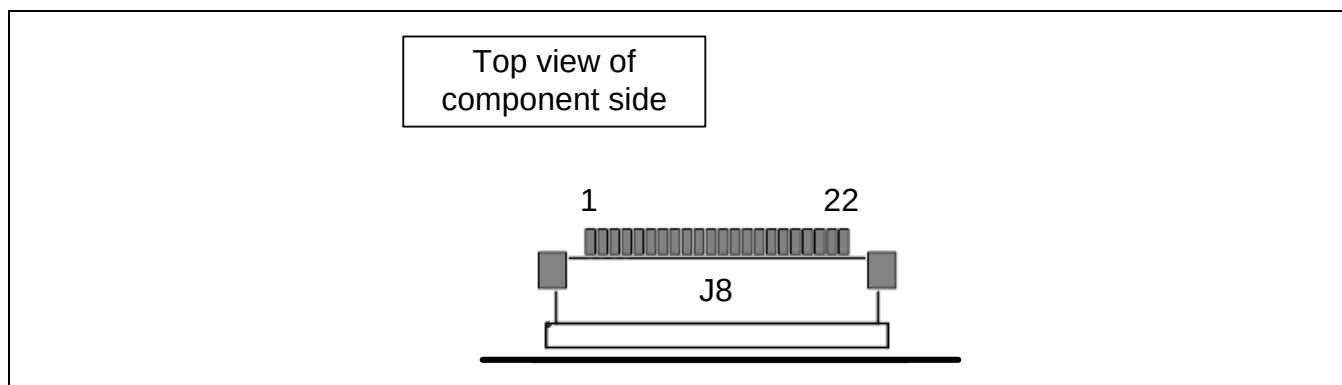


Figure 3.1.10 Pinout Diagram of CD Deck Connector

Table 3.1.14 CD Deck Connector Pin Assignments

Pin No.	Signal Name	Pin No.	Signal Name
1	GND (Vss)	2	GND (Vss)
3	+8V	4	+8V
5	FLAG6 (P1_13 / AN5 / DV0_HSYNC / WAIT)	6	NC
7	CDRST (RES#)	8	GND (Vss)
9	+3.3V	10	+3.3V
11	GND (Vss)	12	CDFS (P3_3 / LCD0_TCON2 / ET_MDIO / IRQ4 / BS / SCI_CTS1 / RTS1 / DACK0 / PWM2D / MISO3)
13	CDSI (P4_2 / LCD0_DATA10 / TI0C0C / FALE / CRx3 / TxD2 / MOSI4 / MMC_D6)	14	CDCK (P4_0 / LCD0_DATA8 / TI0C0A / FRE / RSPCK4 / MMC_D4)
15	CDSO (P4_3 / LCD0_DATA11 / TI0C0D / FWE / CTx3 / RxD2 / MISO4 / MMC_D7)	16	NC
17	IIS_BCK (P3_4 / LCD0_TCON3 / ET_RXCLK / SSI SCK1 / AUDIO_XOUT2 / SCI_SCK0 / TI0C3A / SCK3)	18	IIS_LRCK (P3_5 / LCD0_TCON4 / ET_RXER / SSI WS1 / AUDIO_XOUT3 / SCI_TXD0 / TI0C3B / TxD3)
19	IIS_DATA (P3_6 / LCD0_TCON5 / ET_RXDV / SSI RxD1 / SCI_RXD0 / TI0C3C / RxD3)	20	BLKCK (P3_1 / LCD0_TCON0 / ET_TXER / IRQ6 / TxD2 / SCI_TXD1 / AUDIO_CLK / PWM2B / SSL30)
21	TRANS (P1_12 / AN4 / DV0_VSYNC / VIO_FLD)	22	NC

Note: Bold letters indicate setting functions

3.1.9 LCD Panel Connectors (J10 to J14)

The RTK7721000B00000BR has five connectors (J10 to J14) with three types to connect the LCD panel.

Figure 3.1.11 and Figure 3.1.12 show the Pinout Diagram of LCD Panel Connectors. Table 3.1.15 to Table 3.1.20 list the LCD panel connector Pin Assignments.

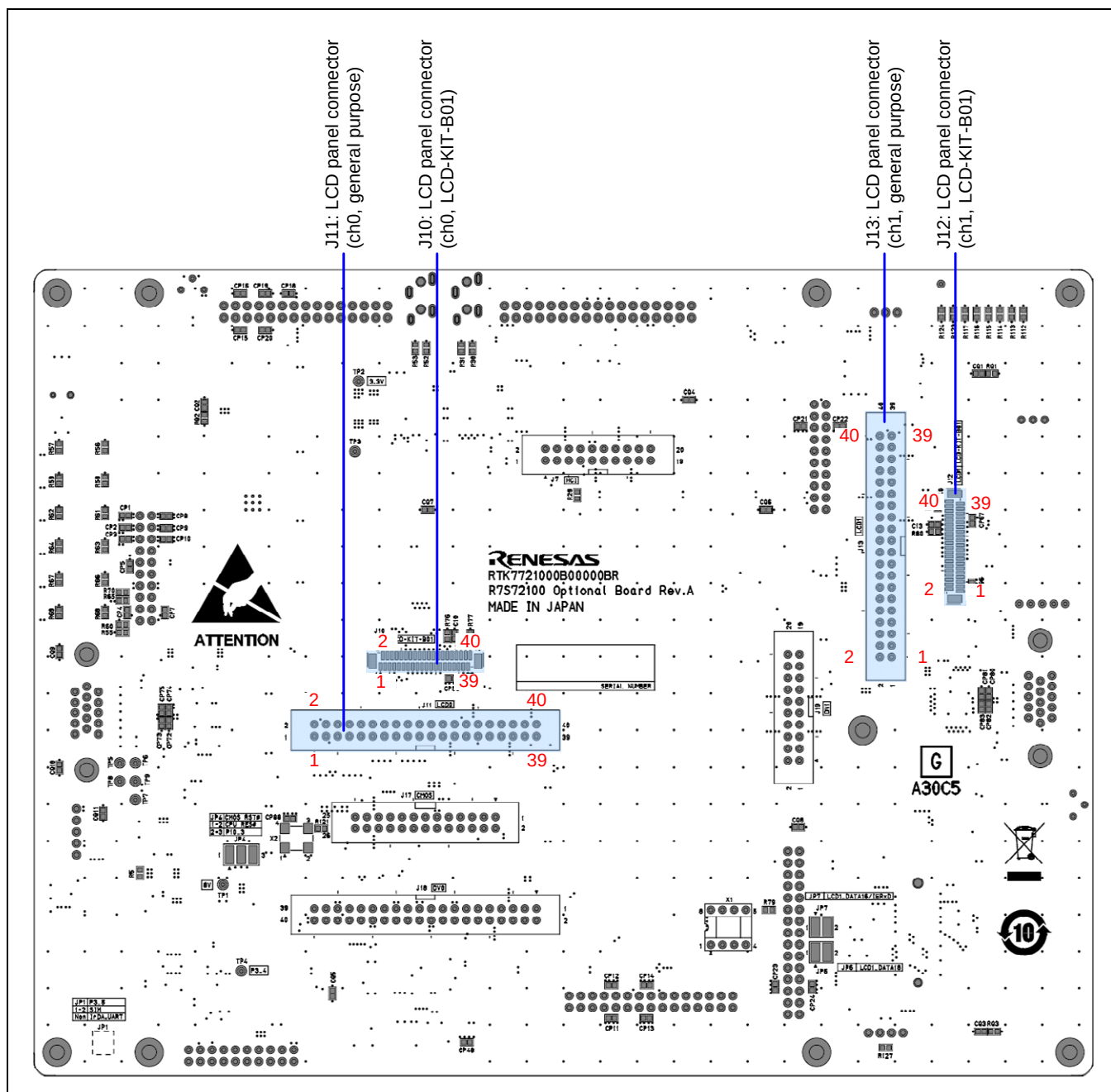


Figure 3.1.11 Pinout Diagram of LCD Panel Connectors 1 (J10 to J13)

Table 3.1.15 LCD Panel Connector Pin Assignments 1 (J10: ch0, For LCD-KIT-B01)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	+3.3V	4	GND (Vss)
5	GND (Vss)	6	B0 (P11_7 / DV0_DATA19 / SD_D0_0 / CTS5 / MMC_D0 / LCD0_DATA0)
7	B1 (P11_6 / DV0_DATA18 / SD_D1_0 / SSIDATA4 / MMC_D1 / LCD0_DATA1)	8	B2 (P11_5 / DV0_DATA17 / SD_WP_0 / SSIWS4 / LCD0_DATA2)
9	B3 (P11_4 / DV0_DATA16 / SD_CD_0 / SSISCK4 / MMC_CD / LCD0_DATA3)	10	B4 (P11_3 / DV0_DATA15 / TIOC4D / LCD0_DATA4 / VIO_D15)
11	B5 (P11_2 / DV0_DATA14 / TIOC4C / RxD6 / LCD0_DATA5 / VIO_D14)	12	GND (Vss)
13	G0 (P11_1 / DV0_DATA13 / TIOC4B / TxD6 / LCD0_DATA6 / VIO_D13)	14	G1 (P11_0 / DV0_DATA12 / TIOC4A / SCK6 / LCD0_DATA7 / VIO_D12)
15	G2 (P10_15 / DV0_DATA11 / SSITxD1 / MISO0 / LCD0_DATA8 / VIO_D11)	16	G3 (P10_14 / DV0_DATA10 / SSIRxD1 / MOSI0 / LCD0_DATA9 / VIO_D10)
17	G4 (P10_13 / DV0_DATA9 / SSIWS1 / SSL00 / LCD0_DATA10 / VIO_D9)	18	G5 (P10_12 / DV0_DATA8 / SSISCK1 / RSPCK0 / LCD0_DATA11 / VIO_D8)
19	R0 (P10_11 / DV0_DATA7 / TIOC2B / ET_RXD3 / LCD0_DATA12 / VIO_D7)	20	R1 (P10_10 / DV0_DATA6 / TIOC2A / ET_RXD2 / LCD0_DATA13 / VIO_D6)
21	R2(P10_9 / DV0_DATA5 / TIOC1B / ET_RXD1 / LCD0_DATA14 / VIO_D5)	22	R3 (P10_8 / DV0_DATA4 / TIOC1A / ET_RXD0 / LCD0_DATA15 / VIO_D4)
23	R4 (P10_7 / DV0_DATA3 / TIOC0D / PWM2H / ET_TXD3 / LCD0_DATA16 / VIO_D3)	24	R5 (P10_6 / DV0_DATA2 / TIOC0C / PWM2G / ET_TXD2 / LCD0_DATA17 / VIO_D2)
25	GND (Vss)	26	DE (P11_12 / CRx1 / RSPCK1 / IRQ3 / MMC_D4 / LCD0_TCON2)
27	HSYNC (P11_11 / DV0_DATA23 / SD_D2_0 / RxD5 / MMC_D2 / LCD0_TCON3)	28	VSYNC (P11_10 / DV0_DATA22 / SD_D3_0 / TxD5 / MMC_D3 / LCD0_TCON4)
29	GND (Vss)	30	LCDCLK (P11_15 / SPDIF_OUT / MISO1 / IRQ1 / MMC_D7 / LCD0_CLK)
31	GND (Vss)	32	+5V
33	+5V	34	+5V
35	NC	36	SDA (P1_1 / SDA0 / DV0_DATA17 / TCLKC / IRQ1 / VIO_HD / DV0_HSYNC)
37	SCL (P1_0 / SCL0 / DV0_DATA16 / TCLKA / IRQ0 / VIO_VD / DV0_VSYNC)	38	INT (P11_13 / CTx1 / SSL10 / LCD0_TCON4 / MMC_D5 / LCD0_TCON1)
39	NC	40	RESET (P11_14 / SPDIF_IN / MOSI1 / LCD0_TCON5 / MMC_D6 / LCD0_TCON0)

Note: Bold letters indicate setting functions

Table 3.1.16 LCD Panel Connector Pin Assignments 2 (J11: ch0, for general purpose)

Pin No.	Signal Name	Pin No.	Signal Name
1	P11_7 / DV0_DATA19 / SD_D0_0 / CTS5 / MMC_D0 / LCD0_DATA0	2	P11_6 / DV0_DATA18 / SD_D1_0 / SSIDATA4 / MMC_D1 / LCD0_DATA1
3	P11_5 / DV0_DATA17 / SD_WP_0 / SSIWS4 / LCD0_DATA2	4	P11_4 / DV0_DATA16 / SD_CD_0 / SSISCK4 / MMC_CD / LCD0_DATA3
5	GND (Vss)	6	P11_3 / DV0_DATA15 / TIOC4D / LCD0_DATA4 / VIO_D15
7	P11_2 / DV0_DATA14 / TIOC4C / RxD6 / LCD0_DATA5 / VIO_D14	8	P11_1 / DV0_DATA13 / TIOC4B / TxD6 / LCD0_DATA6 / VIO_D13
9	P11_0 / DV0_DATA12 / TIOC4A / SCK6 / LCD0_DATA7 / VIO_D12	10	GND (Vss)
11	P10_15 / DV0_DATA11 / SSITxD1 / MISO0 / LCD0_DATA8 / VIO_D11	12	P10_14 / DV0_DATA10 / SSIRxD1 / MOSI0 / LCD0_DATA9 / VIO_D10
13	P10_13 / DV0_DATA9 / SSIWS1 / SSL00 / LCD0_DATA10 / VIO_D9	14	P10_12 / DV0_DATA8 / SSISCK1 / RSPCK0 / LCD0_DATA11 / VIO_D8
15	GND (Vss)	16	P10_11 / DV0_DATA7 / TIOC2B / ET_RXD3 / LCD0_DATA12 / VIO_D7
17	P10_10 / DV0_DATA6 / TIOC2A / ET_RXD2 / LCD0_DATA13 / VIO_D6	18	P10_9 / DV0_DATA5 / TIOC1B / ET_RXD1 / LCD0_DATA14 / VIO_D5
19	P10_8 / DV0_DATA4 / TIOC1A / ET_RXD0 / LCD0_DATA15 / VIO_D4	20	GND (Vss)
21	P10_7 / DV0_DATA3 / TIOC0D / PWM2H / ET_TXD3 / LCD0_DATA16 / VIO_D3	22	P10_6 / DV0_DATA2 / TIOC0C / PWM2G / ET_TXD2 / LCD0_DATA17 / VIO_D2
23	P10_5 / DV0_DATA1 / TIOC0B / PWM2F / ET_TXD1 / LCD0_DATA18 / VIO_D1	24	P10_4 / DV0_DATA0 / TIOC0A / PWM2E / ET_TXD0 / LCD0_DATA19 / VIO_D0
25	+3.3V	26	P10_3 / TCLKD / PWM2D / ET_CRS / LCD0_DATA20 / VIO_FLD
27	P10_2 / DV0_HSYNC / TCLKC / PWM2C / ET_TXEN / LCD0_DATA21 / VIO_HD	28	P10_1 / DV0_VSYNC / TCLKB / PWM2B / ET_TXER / LCD0_DATA22 / VIO_VD
29	P10_0 / DV0_CLK / TCLKA / PWM2A / ET_TXCLK / LCD0_DATA23 / VIO_CLK	30	+3.3V
31	P11_14 / SPDIF_IN / MOSI1 / LCD0_TCON5 / MMC_D6 / LCD0_TCON0	32	P11_13 / CTx1 / SSL10 / LCD0_TCON4 / MMC_D5 / LCD0_TCON1
33	P11_12 / CRx1 / RSPCK1 / IRQ3 / MMC_D4 / LCD0_TCON2	34	P11_11 / DV0_DATA23 / SD_D2_0 / RxD5 / MMC_D2 / LCD0_TCON3
35	+5V	36	P11_10 / DV0_DATA22 / SD_D3_0 / TxD5 / MMC_D3 / LCD0_TCON4
37	P11_9 / DV0_DATA21 / SD_CMD_0 / SCK5 / MMC_CMD / LCD0_TCON5	38	P11_8 / DV0_DATA20 / SD_CLK_0 / RTS5 / MMC_CLK / LCD0_TCON6
39	P11_15 / SPDIF_OUT / MISO1 / IRQ1 / MMC_D7 / LCD0_CLK	40	+5V

Note: Bold letters indicate setting functions

Table 3.1.17 LCD Panel Connector Pin Assignments 3 (J12: ch1, For LCD-KIT-B01)

Pin No.	Signal Name	Pin No.	Signal Name
1	+3.3V	2	+3.3V
3	+3.3V	4	GND (Vss)
5	GND (Vss)	6	B0 (P5_0 / TXCLKOUTP / LCD1_DATA0 / LCD0_DATA16 / DV1_DATA0 / TxD4 / TIOC0A / RSPCK3)
7	B1 (P5_1 / TXCLKOUTM / LCD1_DATA1 / LCD0_DATA17 / DV1_DATA1 / RxD4 / TIOC0B / SSL30)	8	B2 (P5_2 / TXOUT2P / LCD1_DATA2 / LCD0_DATA18 / DV1_DATA2 / SCK3 / TIOC1B / MOSI3)
9	B3 (P5_3 / TXOUT2M / LCD1_DATA3 / LCD0_DATA19 / DV1_DATA3 / TxD3 / TIOC3C / MISO3)	10	B4 (P5_4 / TXOUT1P / LCD1_DATA4 / LCD0_DATA20 / DV1_DATA4 / RxD3 / TIOC3D / DV0_DATA12)
11	B5 (P5_5 / TXOUT1M / LCD1_DATA5 / LCD0_DATA21 / DV1_DATA5 / AUDIO_XOUT / TIOC0C / FCE / DV0_DATA13)	12	GND (Vss)
13	G0 (P5_6 / TXOUT0P / LCD1_DATA6 / LCD0_DATA22 / DV1_DATA6 / TxD6 / IRQ6 / SPDIF_IN / DV0_DATA14)	14	G1 (P5_7 / TXOUT0M / LCD1_DATA7 / LCD0_DATA23 / DV1_DATA7 / RxD6 / TIOC0D / SPDIF_OUT / DV0_DATA15)
15	G2 (P2_8 / D24 / ET_RXD0 / DV0_DATA8 / SSISCK0 / LCD0_TCON6 / LCD1_DATA8 / VIO_D8 / RSPCK4)	16	G3 (P2_9 / D25 / ET_RXD1 / DV0_DATA9 / SSIWS0 / LRXD0 / LCD1_DATA9 / VIO_D9 / SSL40)
17	G4 (P2_10 / D26 / ET_RXD2 / DV0_DATA10 / SSIRxD0 / LTXD0 / LCD1_DATA10 / VIO_D10 / MOSI4)	18	G5 (P2_11 / D27 / ET_RXD3 / DV0_DATA11 / SSITxD0 / TIOC1A / LCD1_DATA11 / VIO_D11 / MISO4)
19	R0 (P2_12 / D28 / RSPCK0 / DV0_DATA12 / SPBIO01_0 / CRx3 / IRQ6 / LCD1_DATA12 / TIOC1B)	20	R1 (P2_13 / D29 / SSL00 / DV0_DATA13 / SPBIO11_0 / CTx3 / SCK0 / LCD1_DATA13 / IRQ7)
21	R2 (P2_14 / D30 / MOSI0 / DV0_DATA14 / SPBIO21_0 / CRx4 / TxD0 / LCD1_DATA14 / IRQ0)	22	R3 (P2_15 / D31 / MISO0 / DV0_DATA15 / SPBIO31_0 / CAN_CLK / RxD0 / LCD1_DATA15 / IRQ1)
23	R4 (P5_9 / WE2/DQMUL / ET_MDC / DV0_VSYNC / IRQ2 / CRx1 / IERxD / LCD1_DATA16)	24	R5 (P5_10 / WE3/DQMUU/AH / DV0_HSYNC / CTx1 / IETxD / LCD1_DATA17)
25	GND (Vss)	26	DE (P4_14 / LCD0_DATA22 / LCD1_TCON1 / SD_D3_0 / MMC_D3 / SPBIO21_1 / SSIRxD3 / TxD2 / IRQ6)
27	HSYNC (P4_13 / LCD0_DATA21 / LCD1_TCON0 / SD_CMD_0 / MMC_CMD / SPBIO11_1 / SSIWS3 / RxD1 / IRQ5)	28	VSYNC (P4_15 / LCD0_DATA23 / LCD1_TCON2 / SD_D2_0 / MMC_D2 / SPBIO31_1 / SSITxD3 / RxD2 / IRQ7)
29	GND (Vss)	30	LCDCLK (P4_12 / LCD0_DATA20 / LCD1_CLK / SD_CLK_0 / MMC_CLK / SPBIO10_1 / SSISCK3 / TxD1 / IRQ4)
31	GND (Vss)	32	+5V
33	+5V	34	+5V
35	NC	36	SDA (P1_7 / SDA3 / DV1_HSYNC / LRXD0 / IRQ7 / VIO_D13 / DV0_DATA13)
37	SCL (P1_6 / SCL3 / DV1_VSYNC / IERxD / IRQ6 / VIO_D12 / DV0_DATA12)	38	INT (P4_8 / LCD0_DATA16 / LCD1_TCON3 / SD_CD_0 / MMC_CD / SSISCK5 / CTx2 / SCK0 / IRQ0)
39	NC	40	RESET (P4_9 / LCD0_DATA17 / LCD1_TCON4 / SD_WP_0 / SSIWS5 / CRx2 / TxD0 / IRQ1)

Note: Bold letters indicate setting functions

Table 3.1.18 LCD Panel Connector Pin Assignments 4 (J13: ch1, for general purpose)

Pin No.	Signal Name	Pin No.	Signal Name
1	P5_0 / TXCLKOUTP / LCD1_DATA0 / LCD0_DATA16 / DV1_DATA0 / TxD4 / TIOC0A / RSPCK3	2	P5_1 / TXCLKOUTM / LCD1_DATA1 / LCD0_DATA17 / DV1_DATA1 / RxD4 / TIOC0B / SSL30
3	P5_2 / TXOUT2P / LCD1_DATA2 / LCD0_DATA18 / DV1_DATA2 / SCK3 / TIOC1B / MOSI3	4	P5_3 / TXOUT2M / LCD1_DATA3 / LCD0_DATA19 / DV1_DATA3 / TxD3 / TIOC3C / MISO3
5	GND (Vss)	6	P5_4 / TXOUT1P / LCD1_DATA4 / LCD0_DATA20 / DV1_DATA4 / RxD3 / TIOC3D / DV0_DATA12
7	P5_5 / TXOUT1M / LCD1_DATA5 / LCD0_DATA21 / DV1_DATA5 / AUDIO_XOUT / TIOC0C / FCE / DV0_DATA13	8	P5_6 / TXOUT0P / LCD1_DATA6 / LCD0_DATA22 / DV1_DATA6 / TxD6 / IRQ6 / SPDIF_IN / DV0_DATA14
9	P5_7 / TXOUT0M / LCD1_DATA7 / LCD0_DATA23 / DV1_DATA7 / RxD6 / TIOC0D / SPDIF_OUT / DV0_DATA15	10	GND (Vss)
11	P2_8 / D24 / ET_RXD0 / DV0_DATA8 / SSISCK0 / LCD0_TCON6 / LCD1_DATA8 / VIO_D8 / RSPCK4	12	P2_9 / D25 / ET_RXD1 / DV0_DATA9 / SSIWS0 / LRXD0 / LCD1_DATA9 / VIO_D9 / SSL40
13	P2_10 / D26 / ET_RXD2 / DV0_DATA10 / SSIRxD0 / LTxD0 / LCD1_DATA10 / VIO_D10 / MOSI4	14	P2_11 / D27 / ET_RXD3 / DV0_DATA11 / SSITxD0 / TIOC1A / LCD1_DATA11 / VIO_D11 / MISO4
15	GND (Vss)	16	P2_12 / D28 / RSPCK0 / DV0_DATA12 / SPBIO01_0 / CRx3 / IRQ6 / LCD1_DATA12 / TIOC1B
17	P2_13 / D29 / SSL00 / DV0_DATA13 / SPBIO11_0 / CTx3 / SCK0 / LCD1_DATA13 / IRQ7	18	P2_14 / D30 / MOSI0 / DV0_DATA14 / SPBIO21_0 / CRx4 / TxD0 / LCD1_DATA14 / IRQ0
19	P2_15 / D31 / MISO0 / DV0_DATA15 / SPBIO31_0 / CAN_CLK / RxD0 / LCD1_DATA15 / IRQ1	20	GND (Vss)
21	P5_9 / WE2/DQMUL / ET_MDC / DV0_VSYNC / IRQ2 / CRx1 / IERxD / LCD1_DATA16	22	P5_10 / WE3/DQMUU/AH / DV0_HSYNC / CTx1 / IETxD / LCD1_DATA17
23	P9_2 / LCD1_DATA18 / SPBCLK_0 / LTxD0 / SCK1 / A0	24	P9_3 / LCD1_DATA19 / SPBSSL_0 / TxD1
25	+3.3V	26	P9_4 / LCD1_DATA20 / SPBIO00_0 / RxD1
27	P9_5 / LCD1_DATA21 / SPBIO10_0 / SSISCK2 / CTS1 / CS4	28	P9_6 / LCD1_DATA22 / SPBIO20_0 / SSIWS2 / RTS1 / CS5
29	P9_7 / LCD1_DATA23 / SPBIO30_0 / SSIDATA2 / TIOC1A	30	+3.3V
31	P4_13 / LCD0_DATA21 / LCD1_TCON0 / SD_CMD_0 / MMC_CMD / SPBIO11_1 / SSIWS3 / RxD1 / IRQ5	32	P4_14 / LCD0_DATA22 / LCD1_TCON1 / SD_D3_0 / MMC_D3 / SPBIO21_1 / SSIRxD3 / TxD2 / IRQ6
33	P4_15 / LCD0_DATA23 / LCD1_TCON2 / SD_D2_0 / MMC_D2 / SPBIO31_1 / SSITxD3 / RxD2 / IRQ7	34	P4_8 / LCD0_DATA16 / LCD1_TCON3 / SD_CD_0 / MMC_CD / SSISCK5 / CTx2 / SCK0 / IRQ0
35	+5V	36	P4_9 / LCD0_DATA17 / LCD1_TCON4 / SD_WP_0 / SSIWS5 / CRx2 / TxD0 / IRQ1
37	P4_10 / LCD0_DATA18 / LCD1_TCON5 / SD_D1_0 / MMC_D1 / SSIRxD5 / RxD0 / IRQ2	38	P4_11 / LCD0_DATA19 / LCD1_TCON6 / SD_D0_0 / MMC_D0 / SSITxD5 / CTx4 / SCK1 / IRQ3
39	P4_12 / LCD0_DATA20 / LCD1_CLK / SD_CLK_0 / MMC_CLK / SPBIO10_1 / SSISCK3 / TxD1 / IRQ4	40	+5V

Note: Bold letters indicate setting functions

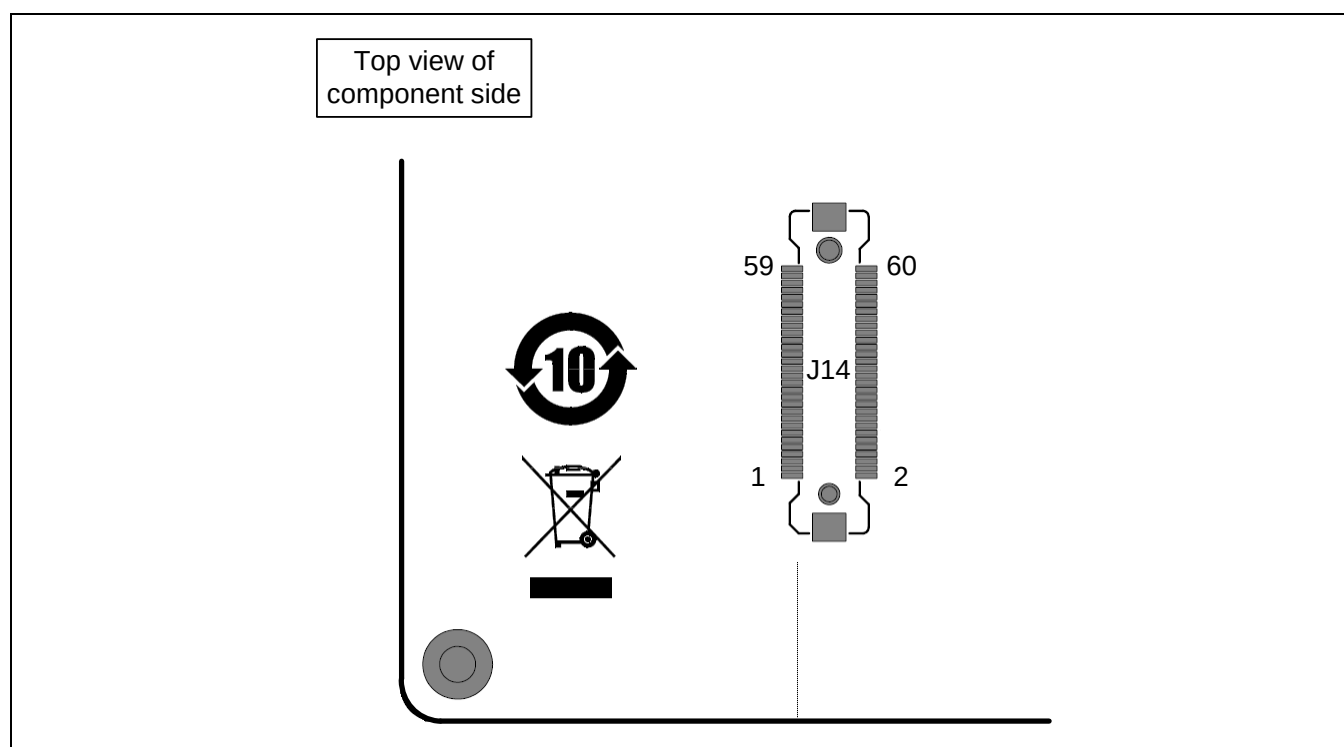


Figure 3.1.12 Pinout Diagram of LCD Panel Connector 2 (J14)

Table 3.1.19 LCD Panel Connector Pin Assignments 5-1 (J14: ch1, For R0P7724LE0011RL)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND (Vss)	2	GND (Vss)
3	LCD0 (P5_0 / TXCLKOUTP / LCD1_DATA0 / LCD0_DATA16 / DV1_DATA0 / TxD4 / TIOC0A / RSPCK3)	4	LCD1 (P5_1 / TXCLKOUTM / LCD1_DATA1 / LCD0_DATA17 / DV1_DATA1 / RxD4 / TIOC0B / SSL30)
5	LCD2 (P5_2 / TXOUT2P / LCD1_DATA2 / LCD0_DATA18 / DV1_DATA2 / SCK3 / TIOC1B / MOSI3)	6	LCD3 (P5_3 / TXOUT2M / LCD1_DATA3 / LCD0_DATA19 / DV1_DATA3 / TxD3 / TIOC3C / MISO3)
7	LCD4 (P5_4 / TXOUT1P / LCD1_DATA4 / LCD0_DATA20 / DV1_DATA4 / RxD3 / TIOC3D / DV0_DATA12)	8	LCD5 (P5_5 / TXOUT1M / LCD1_DATA5 / LCD0_DATA21 / DV1_DATA5 / AUDIO_XOUT / TIOC0C / FCE / DV0_DATA13)
9	LCD6 (P5_6 / TXOUT0P / LCD1_DATA6 / LCD0_DATA22 / DV1_DATA6 / TxD6 / IRQ6 / SPDIF_IN / DV0_DATA14)	10	LCD7 (P5_7 / TXOUT0M / LCD1_DATA7 / LCD0_DATA23 / DV1_DATA7 / RxD6 / TIOC0D / SPDIF_OUT / DV0_DATA15)
11	GND (Vss)	12	GND (Vss)
13	LCD8 (P2_8 / D24 / ET_RXD0 / DV0_DATA8 / SSISCK0 / LCD0_TCON6 / LCD1_DATA8 / VIO_D8 / RSPCK4)	14	LCD9 (P2_9 / D25 / ET_RXD1 / DV0_DATA9 / SSIWS0 / LRXD0 / LCD1_DATA9 / VIO_D9 / SSL40)
15	LCD10 (P2_10 / D26 / ET_RXD2 / DV0_DATA10 / SSIRxD0 / LTxD0 / LCD1_DATA10 / VIO_D10 / MOSI4)	16	LCD11 (P2_11 / D27 / ET_RXD3 / DV0_DATA11 / SSITxD0 / TIOC1A / LCD1_DATA11 / VIO_D11 / MISO4)
17	LCD12 (P2_12 / D28 / RSPCK0 / DV0_DATA12 / SPBIO01_0 / CRx3 / IRQ6 / LCD1_DATA12 / TIOC1B)	18	LCD13 (P2_13 / D29 / SSL00 / DV0_DATA13 / SPBIO11_0 / CTx3 / SCK0 / LCD1_DATA13 / IRQ7)

Note: Bold letters indicate setting functions

Table 3.1.20 LCD Panel Connector Pin Assignments 5-2 (J14: ch1, For R0P7724LE0011RL)

Pin No.	Signal Name	Pin No.	Signal Name
19	LCD14 (P2_14 / D30 / MOSI0 / DV0_DATA14 / SPBIO21_0 / CRx4 / TxD0 / LCD1_DATA14 / IRQ0)	20	LCD15 (P2_15 / D31 / MISO0 / DV0_DATA15 / SPBIO31_0 / CAN_CLK / RxD0 / LCD1_DATA15 / IRQ1)
21	GND (Vss)	22	GND (Vss)
23	LCD16 (P5_9 / WE2/DQMUL / ET_MDC / DV0_VSYNC / IRQ2 / CRx1 / IERxD / LCD1_DATA16)	24	LCD17 (P5_10 / WE3/DQMUU/AH / DV0_HSYNC / CTx1 / IETxD / LCD1_DATA17)
25	LCD18 (P9_2 / LCD1_DATA18 / SPBCLK_0 / LTXD0 / SCK1 / A0)	26	LCD19 (P9_3 / LCD1_DATA19 / SPBSSL_0 / TxD1)
27	LCD20 (P9_4 / LCD1_DATA20 / SPBIO00_0 / RxD1)	28	LCD21 (P9_5 / LCD1_DATA21 / SPBIO10_0 / SSISCK2 / CTS1 / CS4)
29	LCD22 (P9_6 / LCD1_DATA22 / SPBIO20_0 / SSIWS2 / RTS1 / CS5)	30	LCD23 (P9_7 / LCD1_DATA23 / SPBIO30_0 / SSIDATA2 / TIOC1A)
31	GND (Vss)	32	GND (Vss)
33	LCDVSYN (P4_8 / LCD0_DATA16 / LCD1_TCON3 / SD_CD_0 / MMC_CD / SSISCK5 / CTx2 / SCK0 / IRQ0)	34	LCDDISP/RS (P4_10 / LCD0_DATA18 / LCD1_TCON5 / SD_D1_0 / MMC_D1 / SSIRxD5 / RxD0 / IRQ2)
35	LCDHSYN/CS# (P4_9 / LCD0_DATA17 / LCD1_TCON4 / SD_WP_0 / SSIWS5 / CRx2 / TxD0 / IRQ1)	36	NC
37	GND (Vss)	38	GND (Vss)
39	LCDDCK/WR# (P4_12 / LCD0_DATA20 / LCD1_CLK / SD_CLK_0 / MMC_CLK / SPBIO10_1 / SSISCK3 / TxD1 / IRQ4)	40	BKPWM (Connected to +3.3V via 10k Ω resistor)
41	GND (Vss)	42	GND (Vss)
43	LCDDON (Connected to +3.3V via 10k Ω resistor)	44	NC
45	NC	46	GND (Vss)
47	GND (Vss)	48	SDA0 (P1_7 / SDA3 / DV1_HSYNC / LRxD0 / IRQ7 / VIO_D13 / DV0_DATA13)
49	SCL0 (P1_6 / SCL3 / DV1_VSYNC / IERxD / IRQ6 / VIO_D12 / DV0_DATA12)	50	GND (Vss)
51	GND (Vss)	52	TP_IRQ# (P4_11 / LCD0_DATA19 / LCD1_TCON6 / SD_D0_0 / MMC_D0 / SSITxD5 / CTx4 / SCK1 / IRQ3)
53	+3.3V	54	+3.3V
55	+3.3V	56	GND (Vss)
57	GND (Vss)	58	+5V
59	+5V	60	+5V

Note: Bold letters indicate setting functions

3.1.10 Analog RGB Output Connectors (J15 and J16)

The RTK7721000B00000BR has two analog RGB output connectors (J15 and J16).

Figure 3.1.13 shows the Pinout Diagram of analog RGB Output Connectors, and Table 3.1.21 lists the Analog RGB Output Connector Pin Assignments.

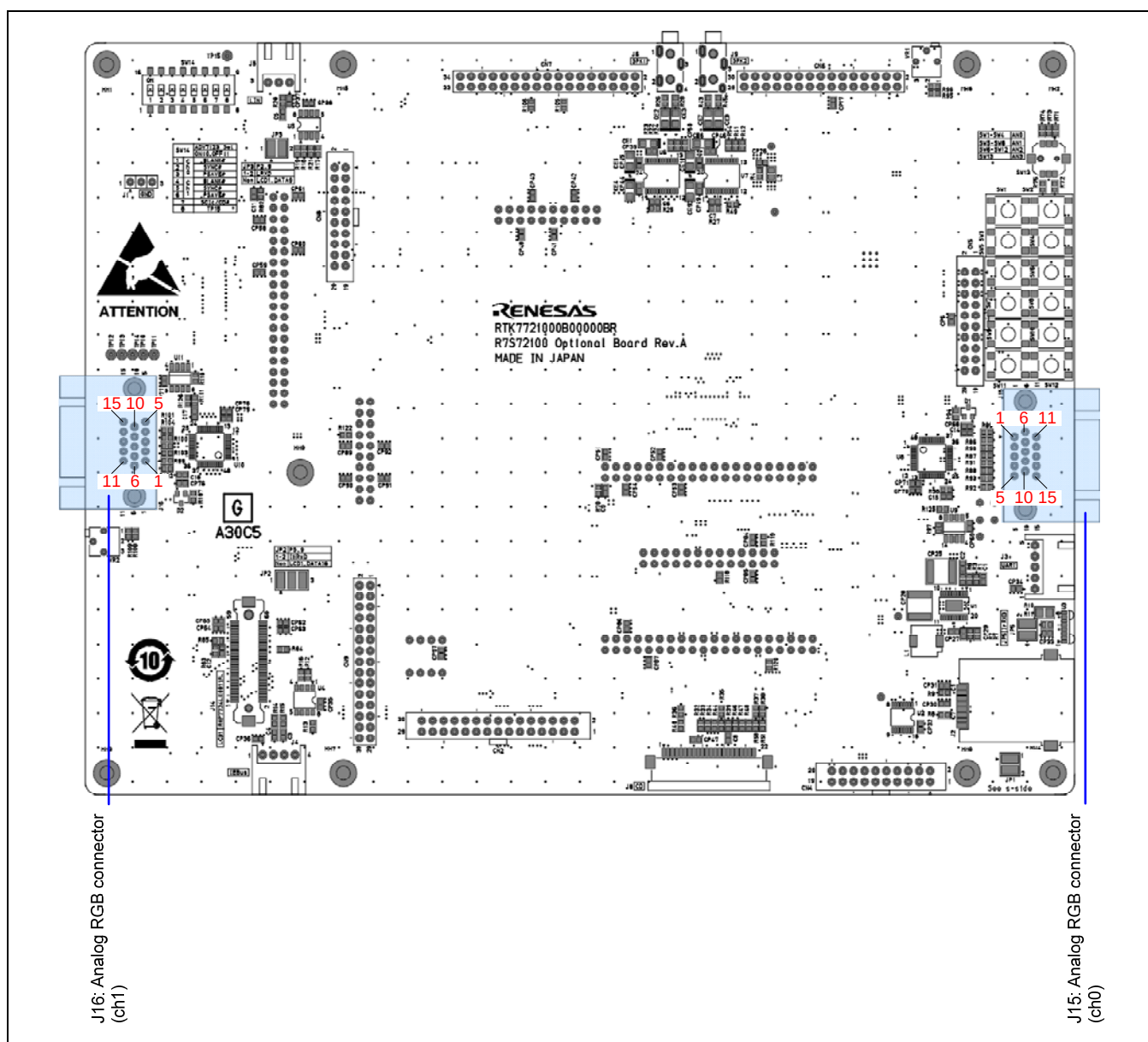


Figure 3.1.13 Pinout Diagram of analog RGB Output Connectors

Table 3.1.21 Analog RGB Output Connector Pin Assignments

Pin No.	Signal Name	
	J15 (ch0)	J16 (ch1)
1	Video signal (Red)	Video signal (Red)
2	Video signal (Green)	Video signal (Green)
3	Video signal (Blue)	Video signal (Blue)
4	NC (Connected to TP5)	NC (Connected to TP10)
5	GND (Vss)	GND (Vss)
6	GND (Vss)	GND (Vss)
7	GND (Vss)	GND (Vss)
8	GND (Vss)	GND (Vss)
9	NC (Connected to TP6)	NC (Connected to TP11)
10	GND (Vss)	GND (Vss)
11	NC (Connected to TP7)	NC (Connected to TP12)
12	SDA (NC: Connected to TP8)	SDA (NC: Connected to TP13)
13	HSYNC (P11_14 / SPDIF_IN / MOSI1 / LCD0_TCON5 / MMC_D6 / LCD0_TCON0)	HSYNC (P4_10 / LCD0_DATA18 / LCD1_TCON5 / SD_D1_0 / MMC_D1 / SSIRxD5 / RxD0 / IRQ2)
14	VSYNC (P11_13 / CTx1 / SSL10 / LCD0_TCON4 / MMC_D5 / LCD0_TCON1)	VSYNC (P4_14 / LCD0_DATA22 / LCD1_TCON1 / SD_D3_0 / MMC_D3 / SPBIO21_1 / SSIRxD3 / TxD2 / IRQ6)
15	SCL (NC: Connected to TP9)	SCL (NC: Connected to TP14)

Note: Bold letters indicate setting functions

3.1.11 CMOS Camera Connector (J17)

The RTK7721000B000000BR has a CMOS camera connector (J17).

Figure 3.1.14 shows the Pinout Diagram of CMOS Camera Connector, and Table 3.1.22 lists the CMOS Camera Connector Pin Assignments.

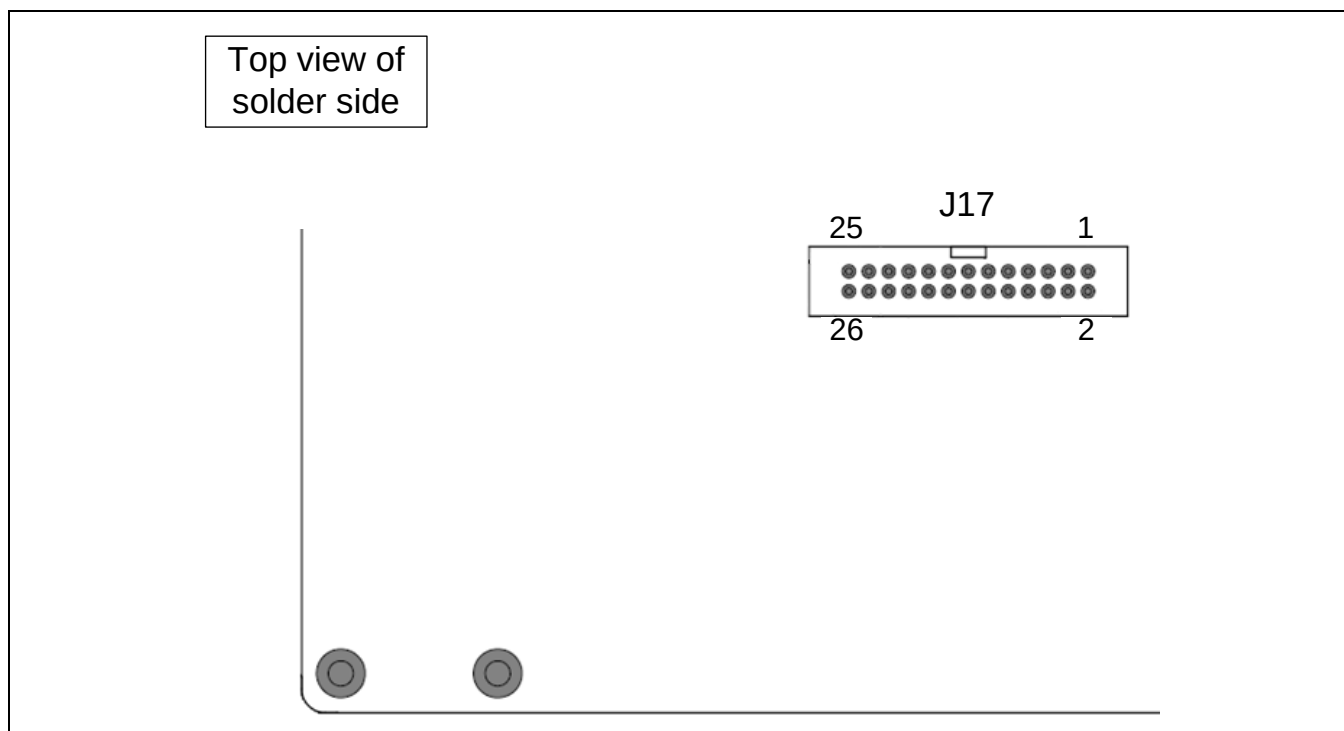


Figure 3.1.14 Pinout Diagram of CMOS Camera Connector

Table 3.1.22 CMOS Camera Connector Pin Assignments

Pin No.	Signal Name	Pin No.	Signal Name
1	S_DOUT0 (P10_6 / DV0_DATA2 / TIOC0C / PWM2G / ET_TXD2 / LCD0_DATA17 / VIO_D2)	2	S_DOUT1 (P10_7 / DV0_DATA3 / TIOC0D / PWM2H / ET_TXD3 / LCD0_DATA16 / VIO_D3)
3	S_DOUT2 (P10_8 / DV0_DATA4 / TIOC1A / ET_RXD0 / LCD0_DATA15 / VIO_D4)	4	S_DOUT3 (P10_9 / DV0_DATA5 / TIOC1B / ET_RXD1 / LCD0_DATA14 / VIO_D5)
5	S_DOUT4 (P10_10 / DV0_DATA6 / TIOC2A / ET_RXD2 / LCD0_DATA13 / VIO_D6)	6	S_DOUT5 (P10_11 / DV0_DATA7 / TIOC2B / ET_RXD3 / LCD0_DATA12 / VIO_D7)
7	S_DOUT6 (P10_12 / DV0_DATA8 / SSISCK1 / RSPCK0 / LCD0_DATA11 / VIO_D8)	8	S_DOUT7 (P10_13 / DV0_DATA9 / SSIWS1 / SSL00 / LCD0_DATA10 / VIO_D9)
9	S_DOUT_LSB0 (P10_4 / DV0_DATA0 / TIOC0A / PWM2E / ET_TXD0 / LCD0_DATA19 / VIO_D0)	10	S_DOUT_LSB1 (P10_5 / DV0_DATA1 / TIOC0B / PWM2F / ET_TXD1 / LCD0_DATA18 / VIO_D1)
11	GND (Vss)	12	GND (Vss)
13	S_LV (P10_2 / DV0_HSYNC / TCLKC / PWM2C / ET_TXEN / LCD0_DATA21 / VIO_HD)	14	NC
15	NC	16	RST (Selects RES# or P10_3 / TCLKD / PWM2D / ET_CRS / LCD0_DATA20 / VIO_FLD at JP4)
17	S_FV (P10_1 / DV0_VSYNC / TCLKB / PWM2B / ET_TXER / LCD0_DATA22 / VIO_VD)	18	SDA (P1_1 / SDA0 / DV0_DATA17 / TCLKC / IRQ1 / VIO_HD / DV0_HSYNC)
19	SCL (P1_0 / SCL0 / DV0_DATA16 / TCLKA / IRQ0 / VIO_VD / DV0_VSYNC)	20	NC
21	+5V	22	+5V
23	S_PIXCLK (P10_0 / DV0_CLK / TCLKA / PWM2A / ET_TXCLK / LCD0_DATA23 / VIO_CLK)	24	GND (Vss)
25	GND (Vss)	26	XMCLK (Connects 27MHz oscillator)

Note: Bold letters indicate setting functions

3.1.12 Digital Video Signal Input Connectors (J18 and J19)

The RTK7721000B00000BR has two digital video signal input connectors (J18 and J19).

Figure 3.1.15 shows the Pinout Diagram of Digital Video Signal Input Connectors. Table 3.1.23 and Table 3.1.24 list the Digital Video Signal Input Pin Assignments.

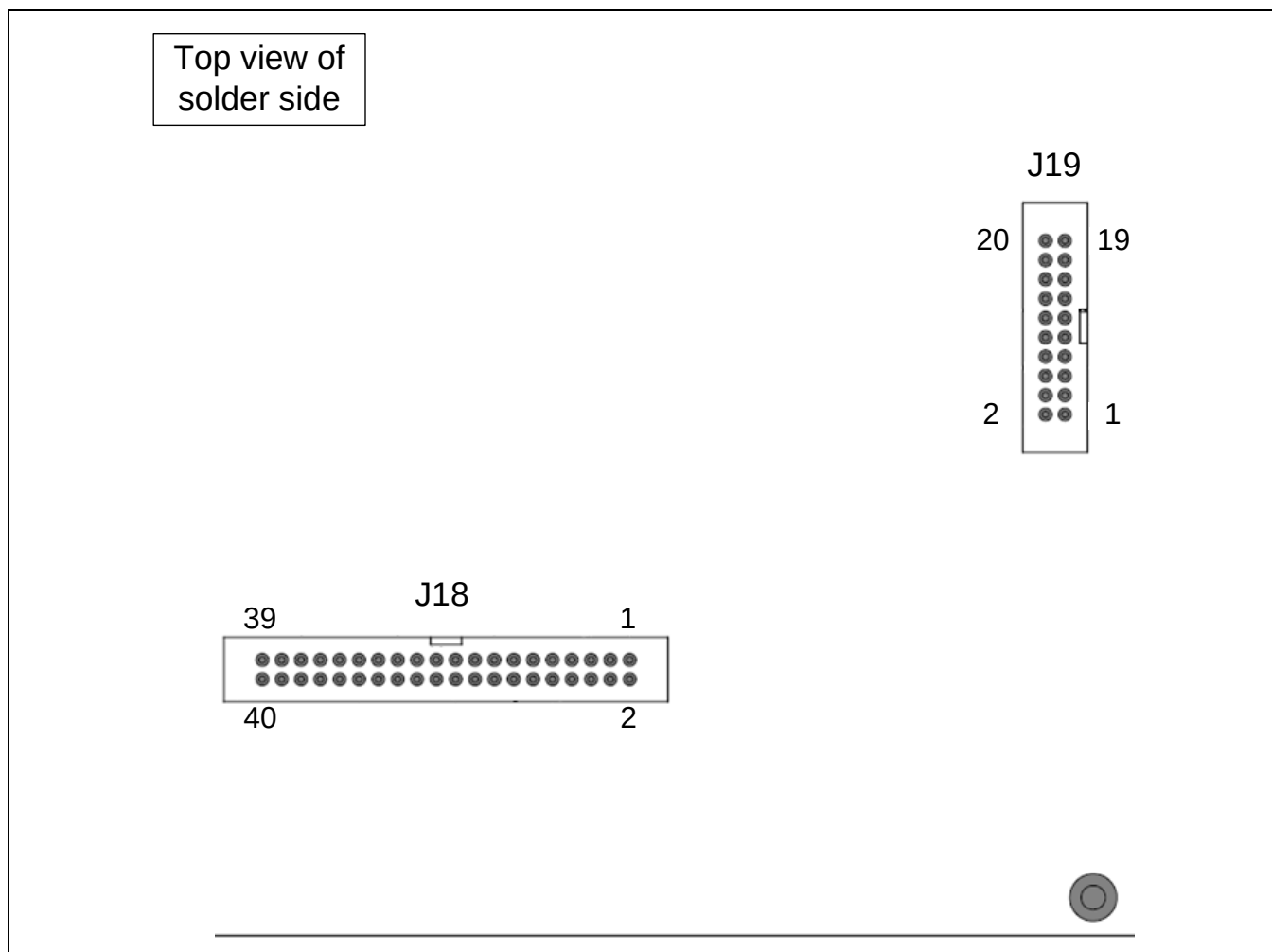


Figure 3.1.15 Pinout Diagram of Digital Video Signal Input Connectors

Table 3.1.23 Digital Video Signal Input Connector Pin Assignments 1 (J18: ch0)

Pin No.	Signal Name	Pin No.	Signal Name
1	P10_4 / DV0_DATA0 / TIOC0A / PWM2E / ET_TXD0 / LCD0_DATA19 / VIO_D0	2	P10_5 / DV0_DATA1 / TIOC0B / PWM2F / ET_TXD1 / LCD0_DATA18 / VIO_D1
3	P10_6 / DV0_DATA2 / TIOC0C / PWM2G / ET_TXD2 / LCD0_DATA17 / VIO_D2	4	P10_7 / DV0_DATA3 / TIOC0D / PWM2H / ET_TXD3 / LCD0_DATA16 / VIO_D3
5	+3.3V	6	P10_8 / DV0_DATA4 / TIOC1A / ET_RXD0 / LCD0_DATA15 / VIO_D4
7	P10_9 / DV0_DATA5 / TIOC1B / ET_RXD1 / LCD0_DATA14 / VIO_D5	8	P10_10 / DV0_DATA6 / TIOC2A / ET_RXD2 / LCD0_DATA13 / VIO_D6
9	P10_11 / DV0_DATA7 / TIOC2B / ET_RXD3 / LCD0_DATA12 / VIO_D7	10	+5V
11	P10_12 / DV0_DATA8 / SSISCK1 / RSPCK0 / LCD0_DATA11 / VIO_D8	12	P10_13 / DV0_DATA9 / SSIWS1 / SSL00 / LCD0_DATA10 / VIO_D9
13	P10_14 / DV0_DATA10 / SSIRxD1 / MOSI0 / LCD0_DATA9 / VIO_D10	14	P10_15 / DV0_DATA11 / SSITxD1 / MISO0 / LCD0_DATA8 / VIO_D11
15	+3.3V	16	P11_0 / DV0_DATA12 / TIOC4A / SCK6 / LCD0_DATA7 / VIO_D12
17	P11_1 / DV0_DATA13 / TIOC4B / TxD6 / LCD0_DATA6 / VIO_D13	18	P11_2 / DV0_DATA14 / TIOC4C / RxD6 / LCD0_DATA5 / VIO_D14
19	P11_3 / DV0_DATA15 / TIOC4D / LCD0_DATA4 / VIO_D15	20	+5V
21	P11_4 / DV0_DATA16 / SD_CD_0 / SSISCK4 / MMC_CD / LCD0_DATA3	22	P11_5 / DV0_DATA17 / SD_WP_0 / SSIWS4 / LCD0_DATA2
23	P11_6 / DV0_DATA18 / SD_D1_0 / SSIDATA4 / MMC_D1 / LCD0_DATA1	24	P11_7 / DV0_DATA19 / SD_D0_0 / CTS5 / MMC_D0 / LCD0_DATA0
25	GND (Vss)	26	P11_8 / DV0_DATA20 / SD_CLK_0 / RTS5 / MMC_CLK / LCD0_TCON6
27	P11_9 / DV0_DATA21 / SD_CMD_0 / SCK5 / MMC_CMD / LCD0_TCON5	28	P11_10 / DV0_DATA22 / SD_D3_0 / TxD5 / MMC_D3 / LCD0_TCON4
29	P11_11 / DV0_DATA23 / SD_D2_0 / RxD5 / MMC_D2 / LCD0_TCON3	30	GND (Vss)
31	NC	32	P10_0 / DV0_CLK / TCLKA / PWM2A / ET_TXCLK / LCD0_DATA23 / VIO_CLK
33	P10_1 / DV0_VSYNC / TCLKB / PWM2B / ET_TXER / LCD0_DATA22 / VIO_VD	34	P10_2 / DV0_HSYNC / TCLKC / PWM2C / ET_TXEN / LCD0_DATA21 / VIO_HD
35	GND (Vss)	36	NC
37	NC	38	NC
39	NC	40	GND (Vss)

Note: Bold letters indicate setting functions

Table 3.1.24 Digital Video Signal Input Connector Pin Assignments 2 (J19: ch1)

Pin No.	Signal Name	Pin No.	Signal Name
1	P5_0 / TXCLKOUTP / LCD1_DATA0 / LCD0_DATA16 / DV1_DATA0 / TxD4 / TIOC0A / RSPCK3	2	P5_1 / TXCLKOUTM / LCD1_DATA1 / LCD0_DATA17 / DV1_DATA1 / RxD4 / TIOC0B / SSL30
3	P5_2 / TXOUT2P / LCD1_DATA2 / LCD0_DATA18 / DV1_DATA2 / SCK3 / TIOC1B / MOSI3	4	P5_3 / TXOUT2M / LCD1_DATA3 / LCD0_DATA19 / DV1_DATA3 / TxD3 / TIOC3C / MISO3
5	+3.3V	6	+3.3V
7	P5_4 / TXOUT1P / LCD1_DATA4 / LCD0_DATA20 / DV1_DATA4 / RxD3 / TIOC3D / DV0_DATA12	8	P5_5 / TXOUT1M / LCD1_DATA5 / LCD0_DATA21 / DV1_DATA5 / AUDIO_XOUT / TIOC0C / FCE / DV0_DATA13
9	P5_6 / TXOUT0P / LCD1_DATA6 / LCD0_DATA22 / DV1_DATA6 / TxD6 / IRQ6 / SPDIF_IN / DV0_DATA14	10	P5_7 / TXOUT0M / LCD1_DATA7 / LCD0_DATA23 / DV1_DATA7 / RxD6 / TIOC0D / SPDIF_OUT / DV0_DATA15
11	+5V	12	+5V
13	P1_5 / SDA2 / DV1_CLK / CRx4 / IRQ5 / VIO_CLK / LCD1_EXTCLK	14	P1_6 / SCL3 / DV1_VSYNC / IERxD / IRQ6 / VIO_D12 / DV0_DATA12
15	NC	16	P1_7 / SDA3 / DV1_HSYNC / LRxD0 / IRQ7 / VIO_D13 / DV0_DATA13
17	GND (Vss)	18	GND (Vss)
19	NC	20	NC

Note: Bold letters indicate setting functions.

3.2 Operation Parts Layout

Figure 3.2.1 and Figure 3.2.2 show the RTK7721000B00000BR Operation Parts Layouts.

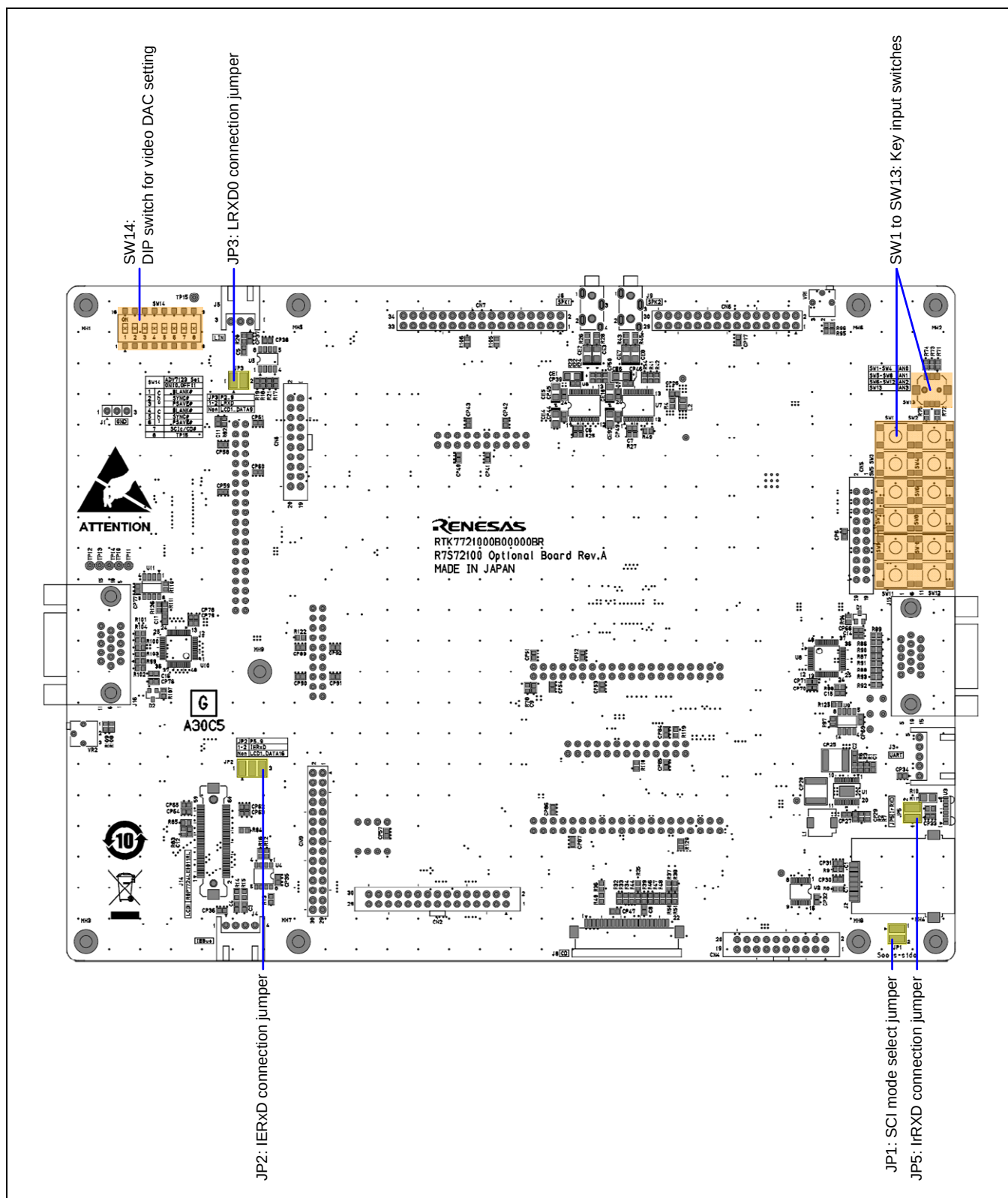


Figure 3.2.1 RTK7721000B00000BR Operation Parts Layout 1 (Top View of Component Side)

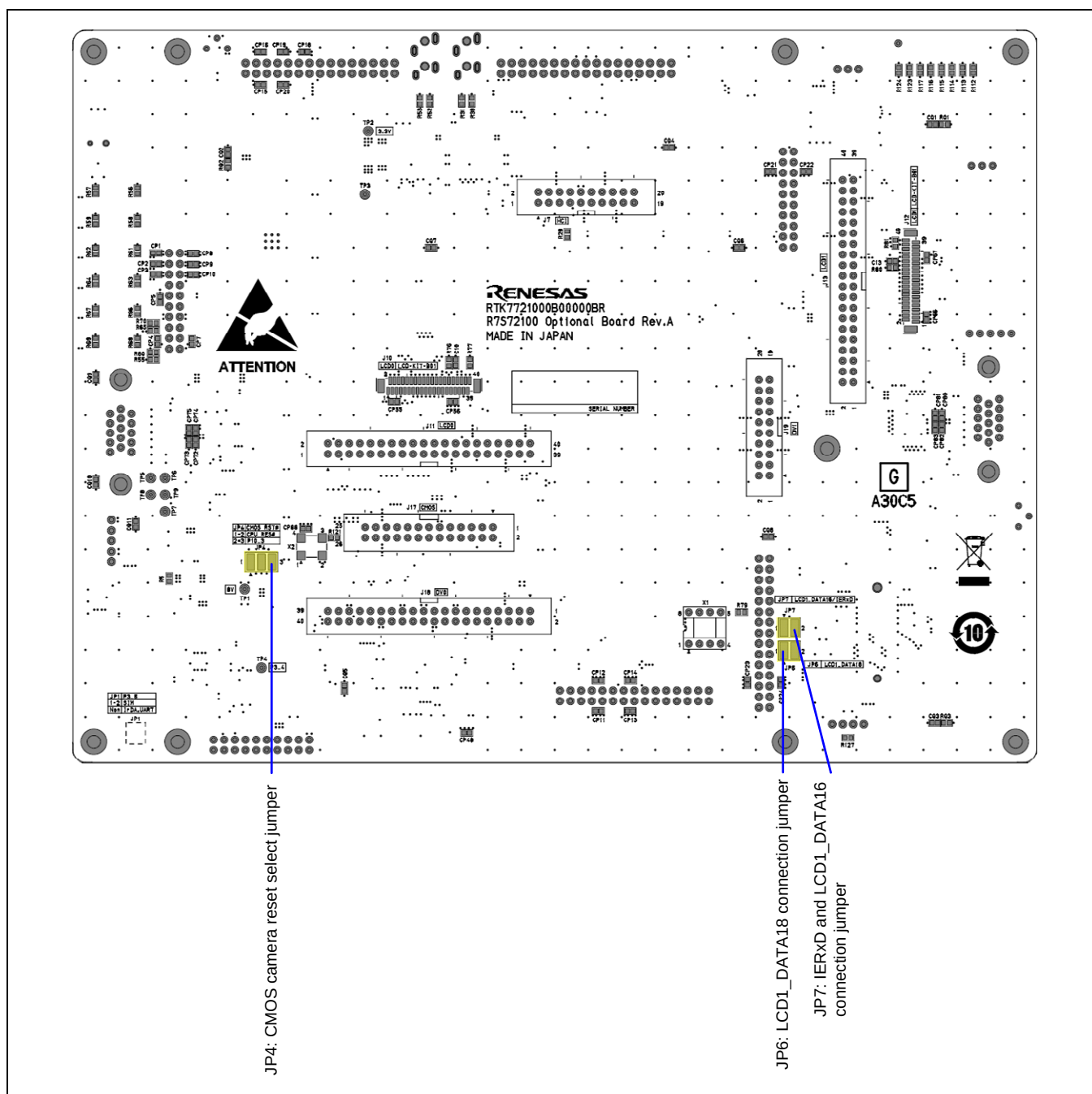


Figure 3.2.2 RTK7721000B00000BR Operation Parts Layout 2 (Top View of Solder Side)

3.2.1 Jumpers (JP1 to JP7)

The RTK7721000B00000BR has seven jumpers for system setting.

Figure 3.2.3 shows the Jumper Layout for RTK7721000B00000BR System Setting, and Table 3.2.1 lists the Jumper Setting for Switching Multifunctional Pins (JP1 to JP7).

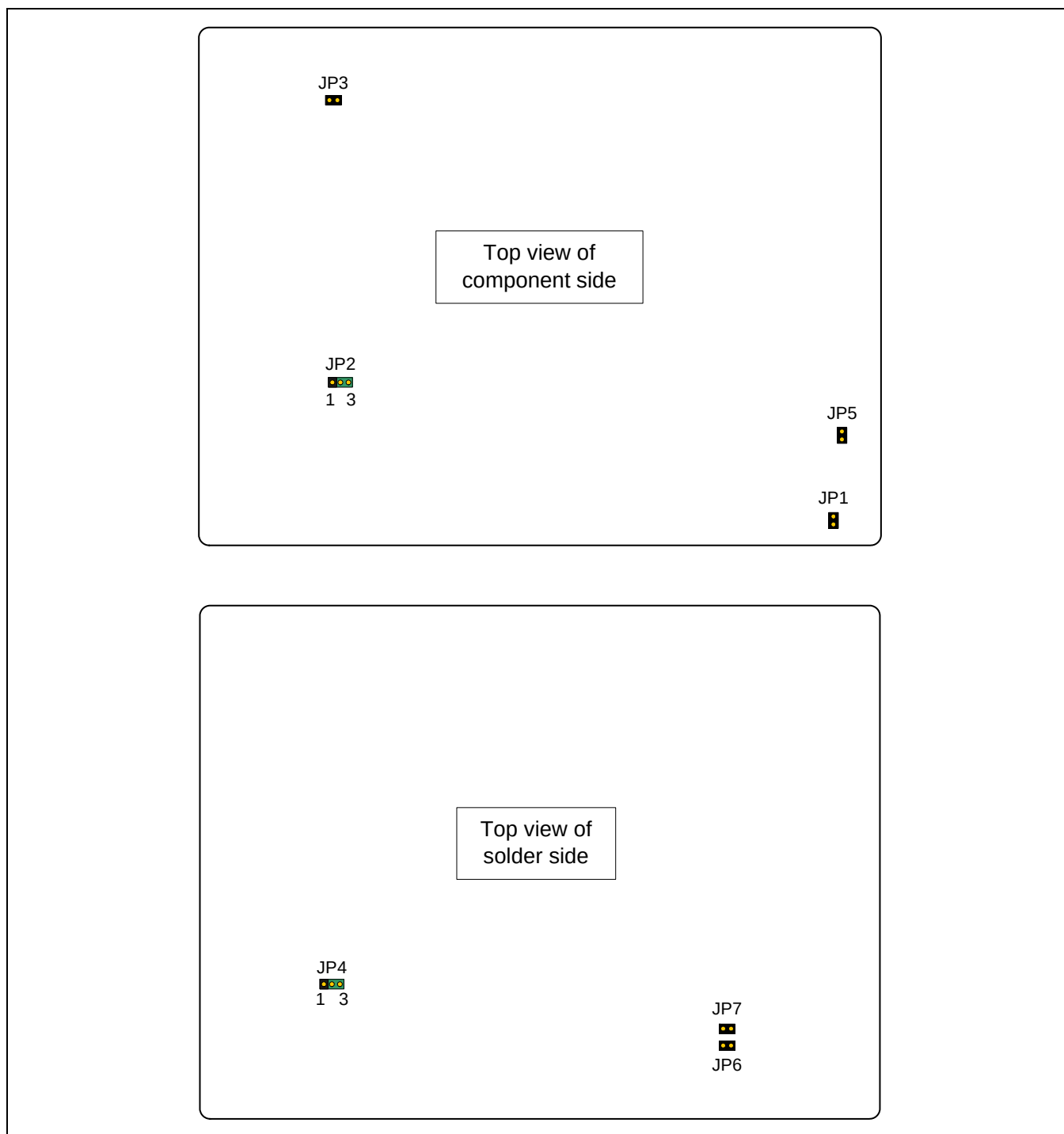


Figure 3.2.3 Jumper Layout for RTK7721000B00000BR System Setting

Table 3.2.1 Jumper Setting for Switching Multifunctional Pins (JP1 to JP7)

Jumper	Setting	Function
JP1 SCI mode select	Short	Connects SCI_TXD0 and SCI_RXD0 as the smart card interface mode
	Open	Disconnects SCI_TXD0 and SCI_RXD0 as the serial communication interface mode
JP2 IERxD / LCD1_DATA16	1 - 2	Connected to IEBus transceiver (U4) as IERxD input pin
	2 - 3	Connected to LCD output connector 2 (J12 to J14) and video DAC 2 (U10) as LCD1_DATA16 output pin
JP3 LRXD0 / LCD1_DATA10	Short	Connected to LIN transceiver (U5) as LRXD0 input pin
	Open	Connected to LCD output connector 2 (J12 to J14) and video DAC 2 (U10) as LCD1_DATA10 output pin
JP4 CMOS camera reset control	1 - 2	Connects RES signal generated on the RTK772100BC00000BR to the reset signal of CMOS camera connector
	2 - 3	Connects P10_3 pin to the reset signal of CMOS camera connector (J17)
JP5 SCI_RXD0/ RxD3	Short	Connected to IrDA module (U3) as SCI_RXD0 input pin
	Open	Connected to SIM card slot (J2) as SCI_RXD0 input pin Connected to UART connector (J3) as RxD3 input pin
JP6 LCD1_DATA18 / SPBCLK_0	Short	Connected to LCD output connector 2 (J12 to J14) and video DAC 2 (U10) as LCD1_DATA18 output pin
	Open	Connected to serial flash memory 1 (U6) and 2 (U7) on the RTK772100BC00000BR as SPBCLK_0 output pin
JP7 ET_MDC / IERxD / LCD1_DATA16	Short	Connected to IEBus transceiver (U4) as IERxD input pin Connected to LCD output connector 2 (J12 to J14) and video DAC 2 (U10) as LCD1_DATA16 output pin
	Open	Connected to Ethernet PHY (U20) on the RTK772100BC00000BR as ET_MDC output pin

 Indicates initial setting.

Note: The power of the board should be off when changing the jumper setting.

3.2.2 Switches

The RTK7721000B00000BR has 14 switches.

Figure 3.2.4 shows the RTK7721000B00000BR Switch Layout. Table 3.2.2 lists the RTK7721000B00000BR Switches, and Table 3.2.3 lists the Function Description of DIP Switch for I/F Setting (SW14).

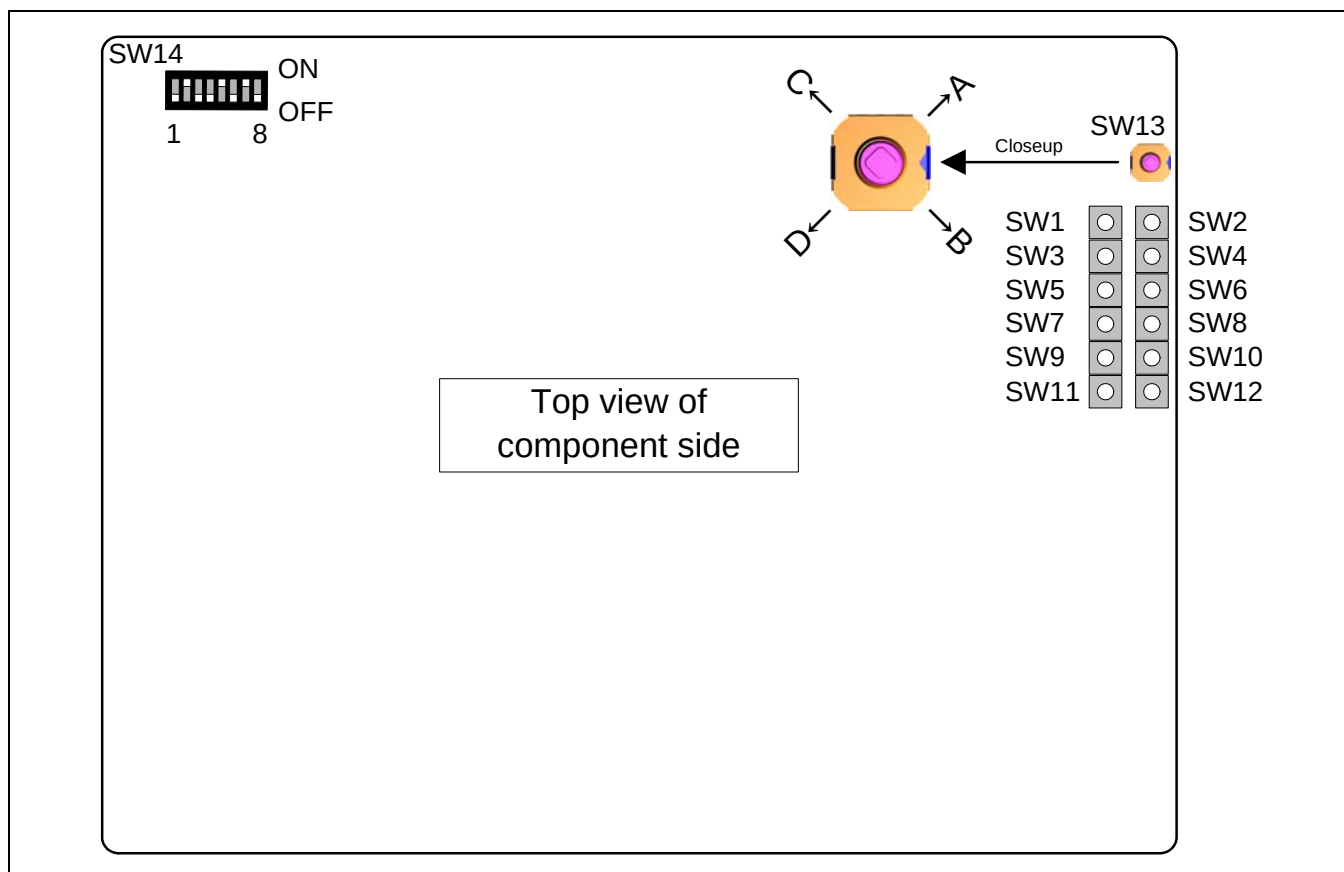


Figure 3.2.4 RTK7721000B00000BR Switch Layout

Table 3.2.2 RTK7721000B00000BR Switches

No.	Function	Remarks
SW1 to SW13	DIP switches for key input	Refer to Section 2.15 for more details
SW14	DIP switch for I/F setting (8/package)	Refer to Table 3.2.3 for more details.

Table 3.2.3 Function Description of DIP Switch for I/F Setting (SW14)

No.	Setting	Function
Video DAC 1	SW14-1 BLANK pin setting	OFF BLANK = "H" Normal analog output
		ON BLANK = "L" Fix analog outputs (IOR, IOB, IOG) to blanking level
	SW14-2 SYNC pin setting	OFF SYNC = "H" Do not remove 40IRE current source
		ON SYNC = "L" Remove 40IRE current source
	SW14-3 PSAVE pin setting	OFF PSAVE = "H" Normal operating mode
		ON PSAVE = "L" Power down mode
Video DAC 2	SW14-4 BLANK pin setting	OFF BLANK = "H" Normal analog output
		ON BLANK = "L" Fix analog outputs (IOR, IOB, IOG) to blanking level
	SW14-5 SYNC pin setting	OFF SYNC = "H" Do not remove 40IRE current source
		ON SYNC = "L" Remove 40IRE current source
	SW14-6 PSAVE pin setting	OFF PSAVE = "H" Normal operating mode
		ON PSAVE = "L" Power down mode
SW14-7 P3_[6:3] selection for connection destination	OFF	SCI# / CD = "H" Connected to CD deck connector (J8)
	ON	SCI# / CD = "L" Connected to SIM card slot (J2), IrDA module (U3) and UART connector (J3)
SW14-8 TP15	OFF	TP15 = "H"
	ON	TP15 = "L"

 Indicates initial setting.

3.3 Dimensions

Figure 3.3.1 and Figure 3.3.2 show the RTK7721000B00000BR Dimensions (Top View of Component Side). Figure 3.3.3 shows the RTK7721000B00000BR Dimensions (Perspective View of Component Side).

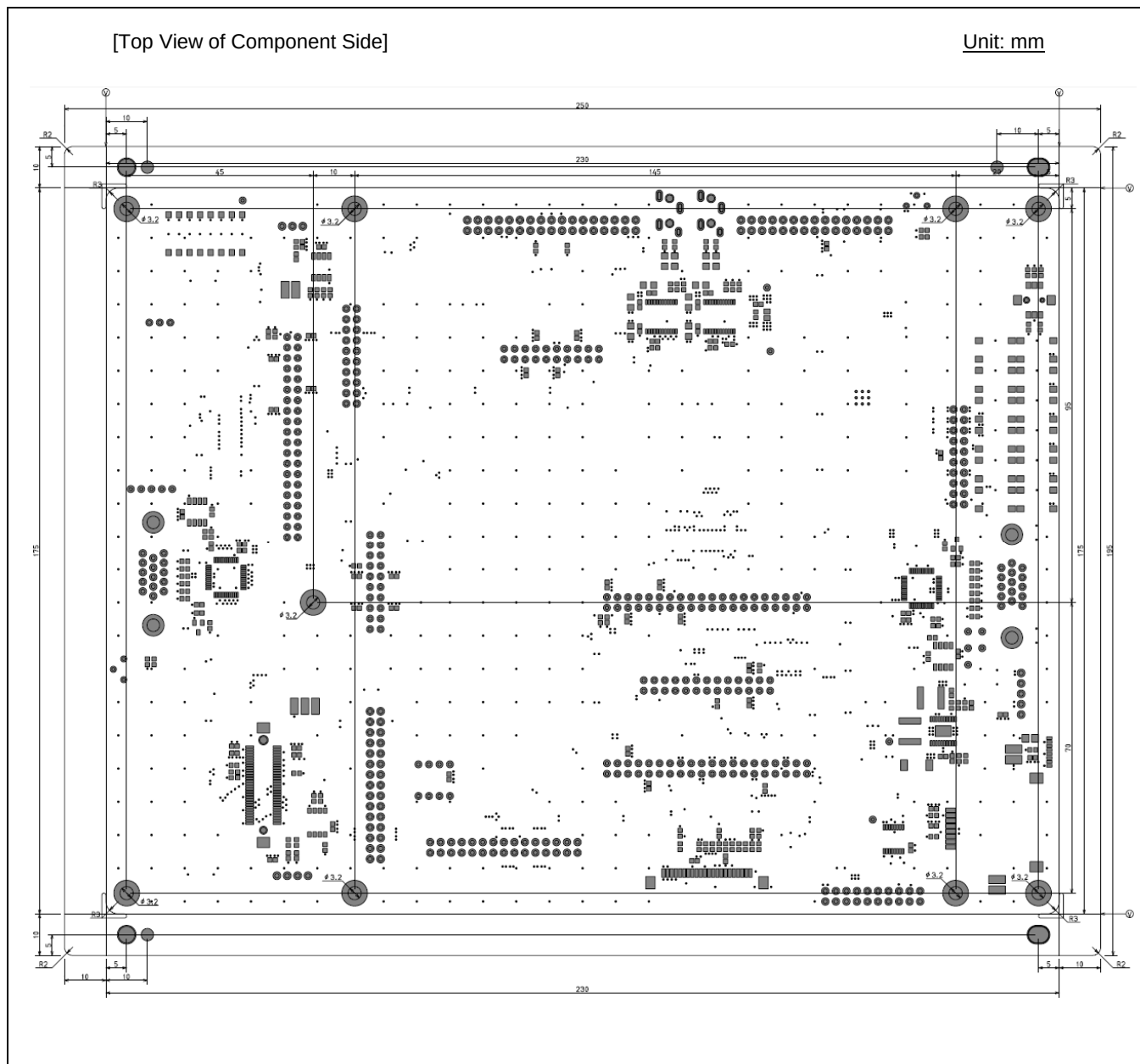


Figure 3.3.1 RTK7721000B00000BR Dimensions 1 (Top View of Component Side1)

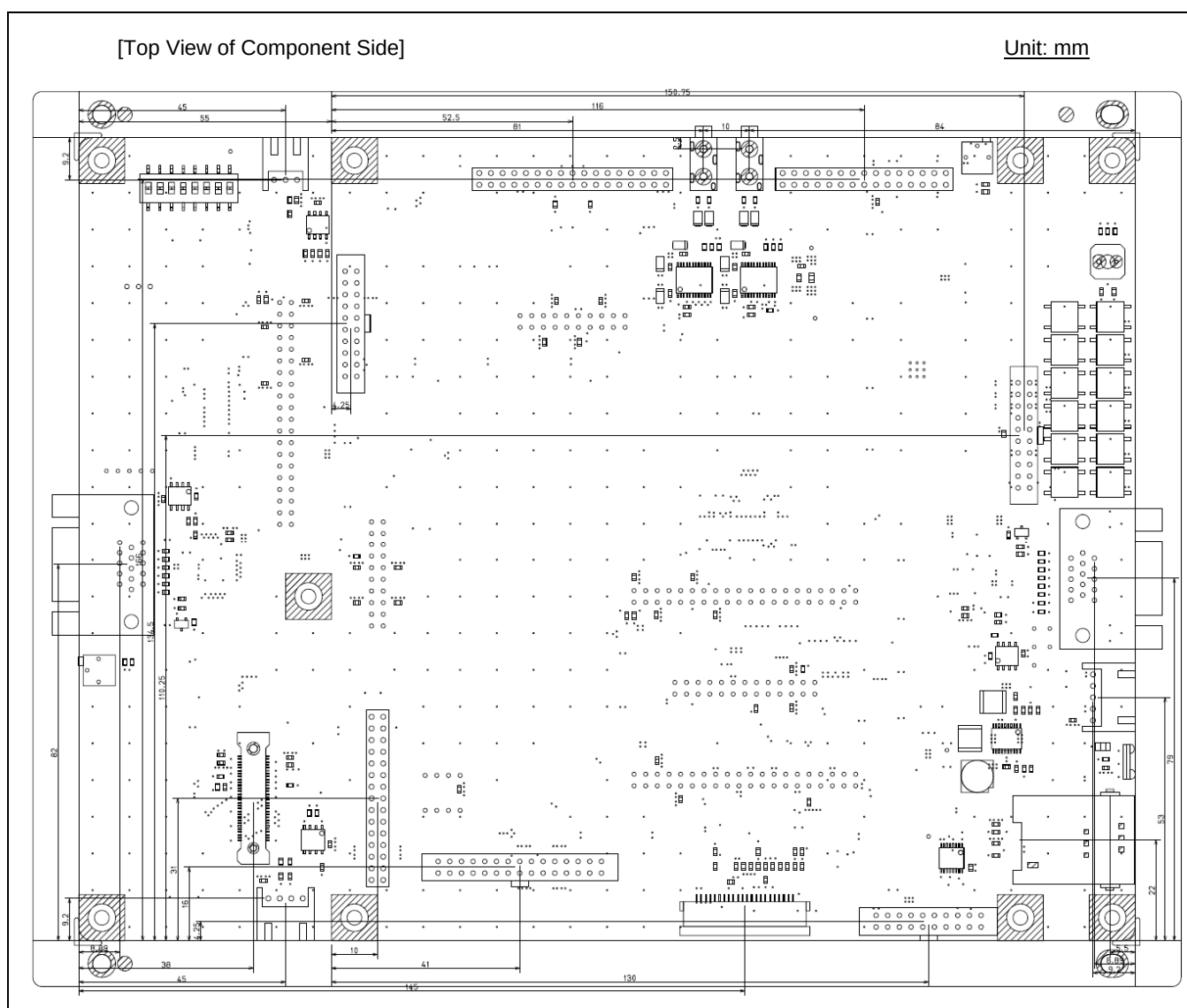


Figure 3.3.2 RTK7721000B00000BR Dimensions 2 (Top View of Component Side 2)

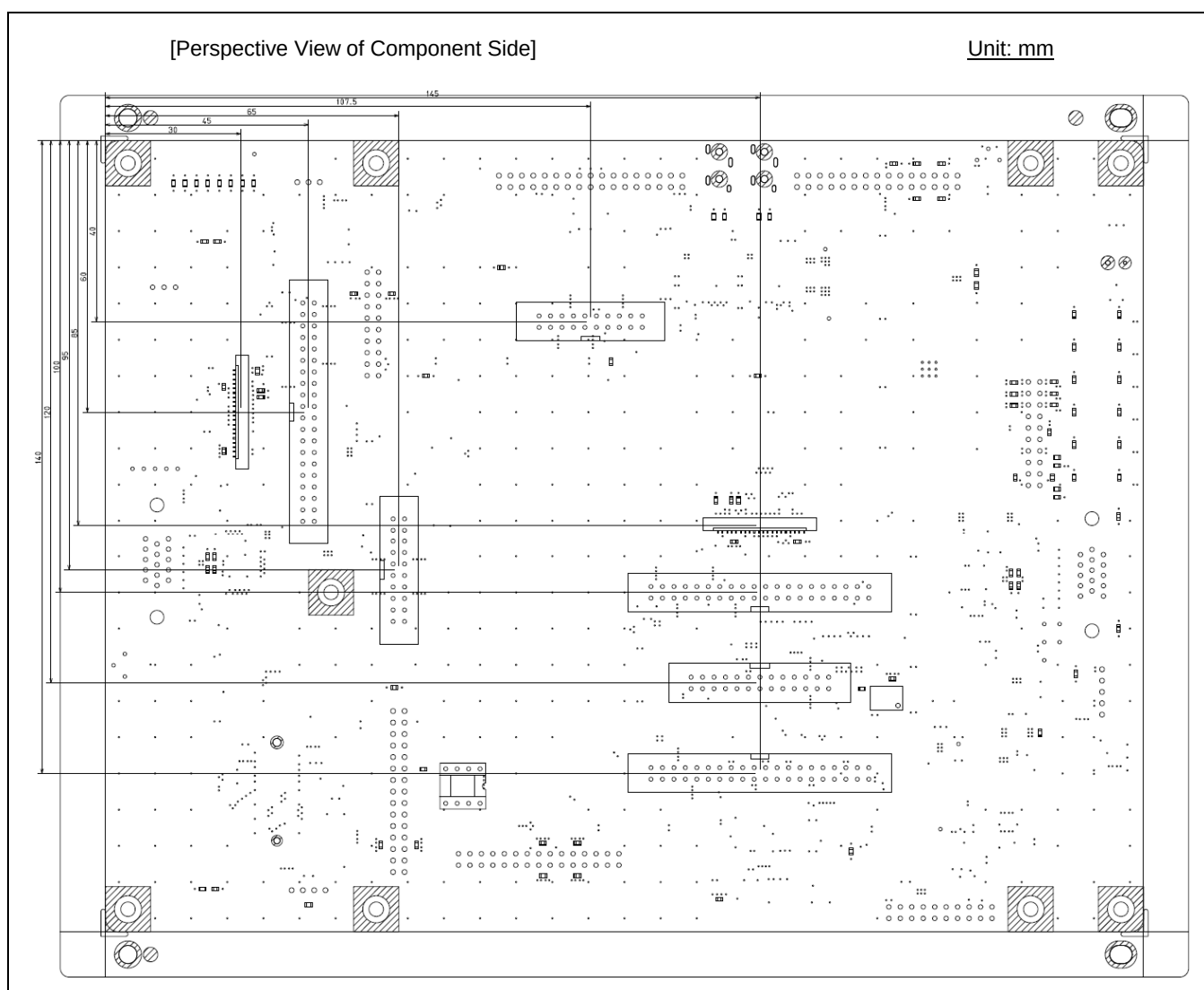


Figure 3.3.3 RTK7721000B00000BR Dimensions 3 (Perspective View of Component Side)

Appendix RTK7721000B000000BR Schematics

R7S72100 Optional board RTK7721000B00000BR SCHEMATICS

for RTK772100FC00000BR & RTK772100BC00000BR

TITLE	PAGE
Index	1
Ext. Connector with CPU board, Power	2
SCiC(SIM, IrDA, UART), IEBus, LIN	3
Audio-DAC, CD, HCI, Push-SW	4
LCD	5
Video-Encoder	6
CMOS, DV	7

Note:

 Digital GND (GND)

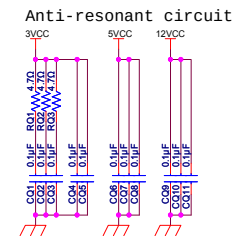
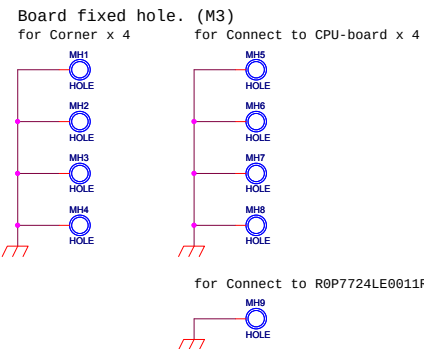
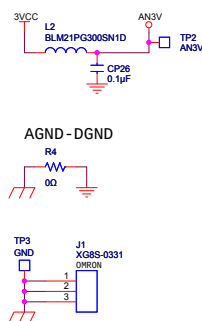
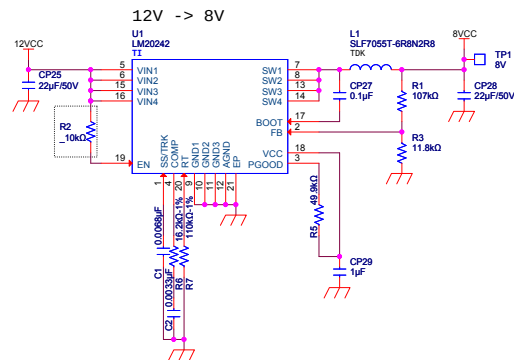
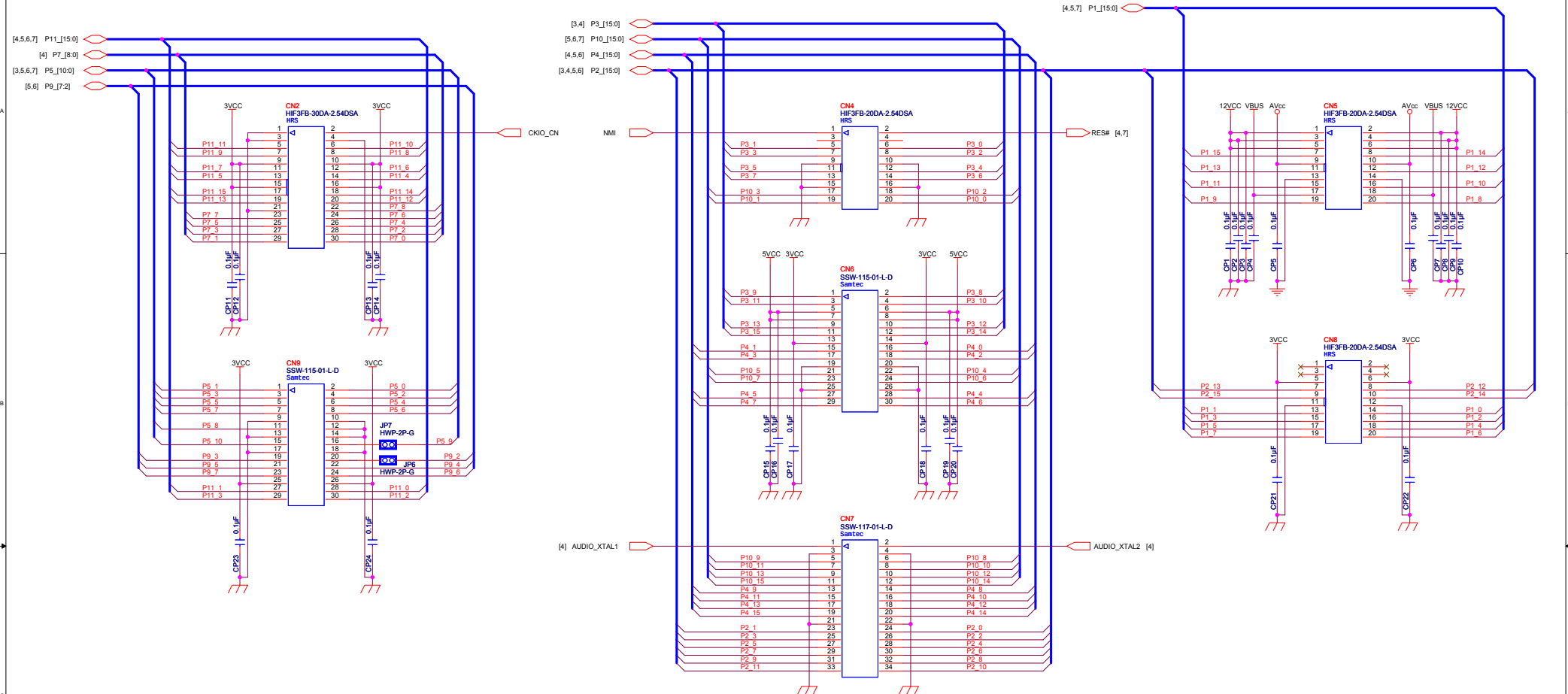
 Analog GND (AVss)

 Not mounted

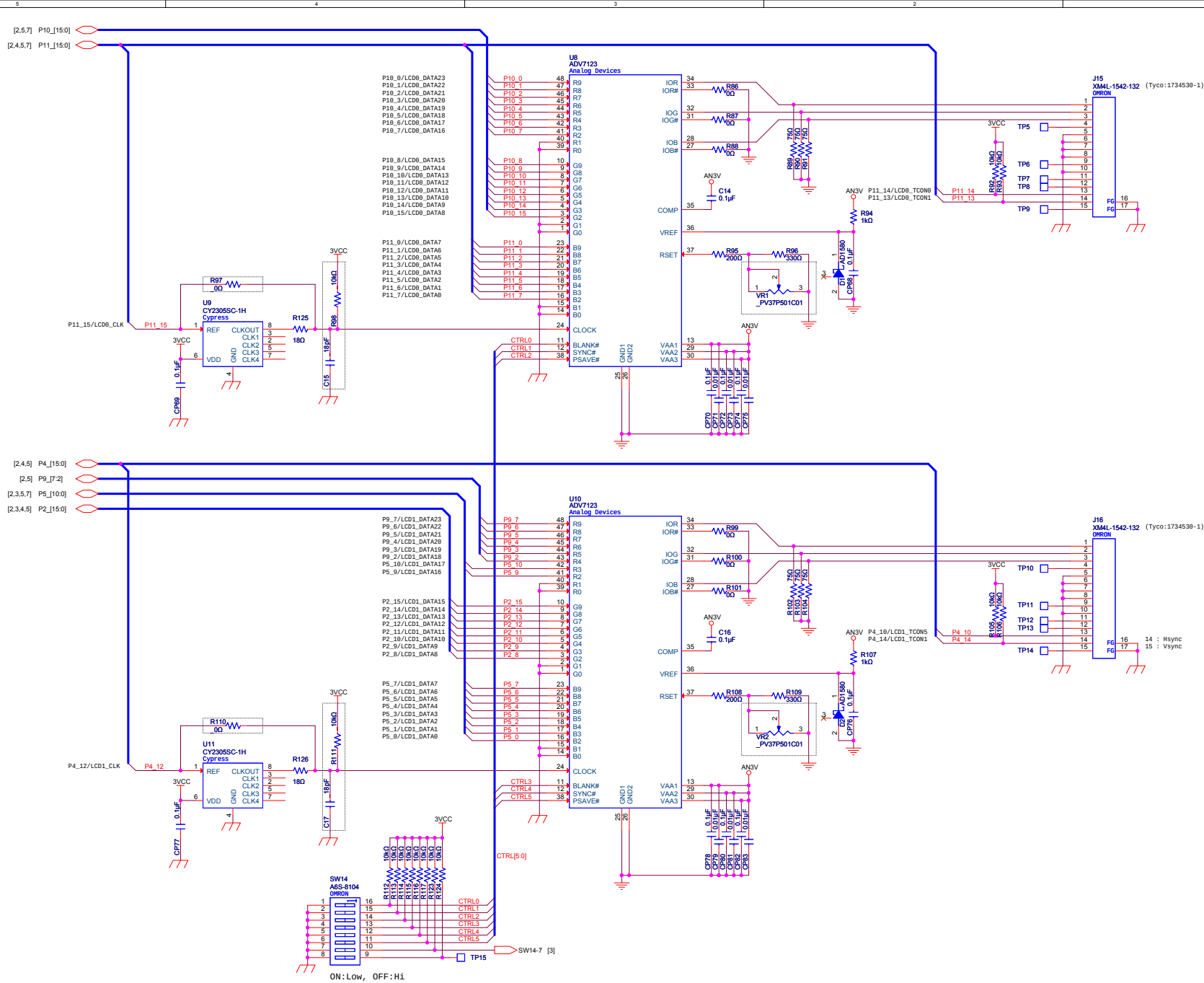
12VCC = Digital 12V (System Power)
8VCC = Digital 8V for CD deck
5VCC = Digital 5V
3VCC = Digital 3.3V
AVcc = Analog 3.3V for R7S72100 ADC
AN3V = Analog 3.3V for AK4353, ADV7123

R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

CHANGE				Renesas Solutions Corp.				RTK7721000B00000BR
		SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	INDEX (1 / 7)
		DATE	13-07-02					D-RTK7721000B00000BR_C-A



CHANGE				Renesas Solutions Corp.				RTK7721000B00000BR
		SCALE		DRAWN	CHECKED	DESIGNED	APPROVED	Ext. Connector, Power (2 / 7)
		DATE	13-07-02					D-RTK7721000B00000BR_C-A



CHANGE				Renesas Solutions Corp.				RTK7721000B00000BR
				DRAWN	CHECKED	DESIGNED	APPROVED	Video Encoder (6 / 7)
		SCALE						
		DATE	13-07-02					D-RTK7721000B00000BR_C-A

REVISION HISTORY	R7S72100 CPU optional board RTK7721000B000000BR User's Manual
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Rev.	Issue date	Description	
		Page	Summary
0.01	Nov. 5, 2012.	-	Preliminary issued
0.02	Nov. 12, 2012	-	Review specifications
0.03	Nov. 16, 2012	-	Correct errors in expansion connectors in the table of pin function
0.04	Jul. 12, 2013	-	Add chapter 1, 3, and cover Correct errors found when deciding details. Check and review the pin names Add general name for the board (GENMAI) Correct errors
0.05	Sep. 06, 2013	-	Correct errors

R7S72100 CPU optional board RTK7721000B00000BR
User's Manual

Publication Date: Sep. 06, 2013 Rev.0.05
Published by: Renesas Electronics Corporation



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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